

15.6" Discrete Block Diagram

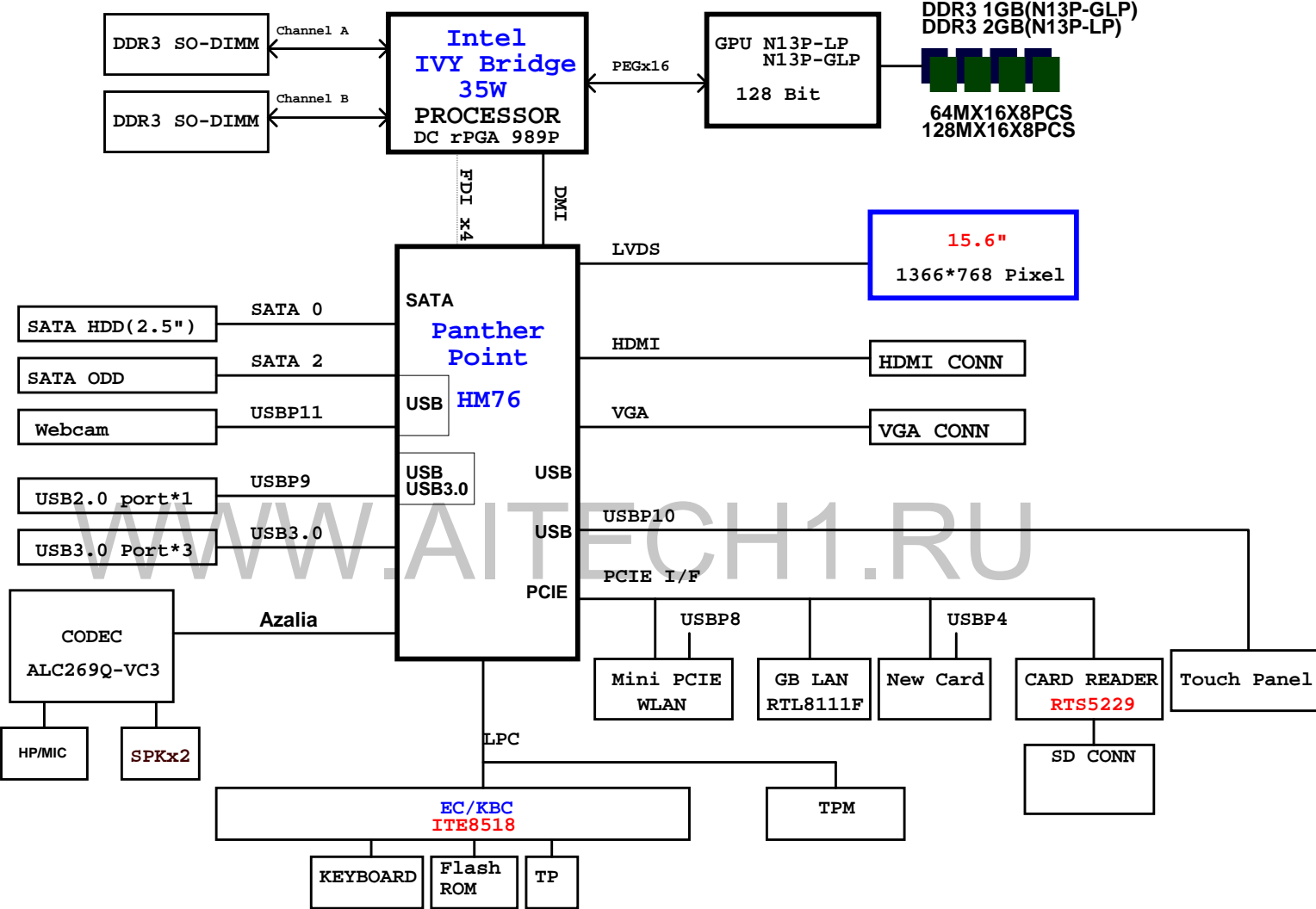
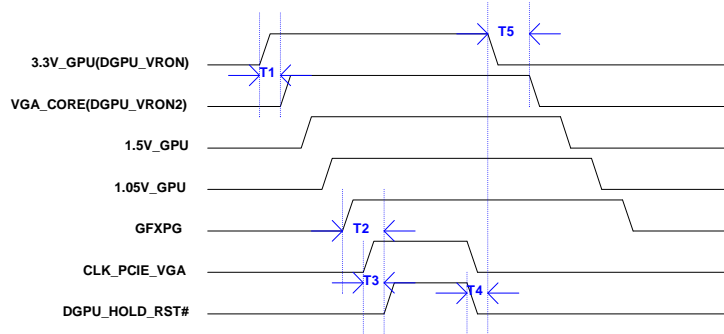


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POWER PLANE	VOLTAGE	CONTROL SIGNAL	Power States ACTIVE IN
VIN	10V~+19V		S0-S5
3V_RTC	+3.0V~+3.3V		S0-G3
3V_S0	+3.3V	S0_ON1	S0
3V_S5	+3.3V	EC	S0-S5
3V_AUX	+3.3V	AC/DC Insert enable	AWLAYS
5V_S0	+5V	S0_ON1	S0
5V_S3	+5V	S3_ON	S0-S3
5V_S5	+5V	EC	S0-S5
5V_AUX	+5V	AC/DC Insert enable	AWLAYS
1.8V_S0	+1.8V	S0_ON2	S0
1.5V_S0	+1.5V	S0_ON2	S0
1.5V_S3	+1.5V	S3_ON	S0-S3
1.05V_S0	+1.05V	S0_ON2	S0
VCCSA	By VID	S0_ON2	S0
CPU_CORE	By VID	VR_ON	S0
VCC_AXG	By VID	VR_ON	S0
3V_LAN	+3.3V	LAN_ON	S0-S5(By WOL)
3V_GPU	+3.3V	DGPU_VRON	Optimus
1.5V_GPU	+1.5V	DGFX_VR_PWRGD	Optimus
1.05V_GPU	+1.05V	DGFX_VR_PWRGD	Optimus
VGA_CORE	By VID	DGPU_VRON1	Optimus

N13P-LP Power ON/OFF Sequence



BIOS/ EC control:

T1:DGPU_VRON to DGPU_VRON2 = 500us

T2:GFXPG to DGPU_HOLD_RST# = 5ms

T3:CLK_PCIE_VGA to DGPU_HOLD_RST# >100us(Spec)

T4:DGPU_HOLD_RST# to DGPU_VRON = 5ms

Note: Clock must be shutdown before 3.3V_GPU

T5:DGPU_VRON to DGPU_VRON2 = 500us

N13P-LP & N13P-GLP Table

	N13P-GLP	N13P-LP
VL3	BLM18P121SN (CX8PG121009)	0ohm_0603 (CS00003J951)

	N13P-GLP	N13P-LP
VR111	NA	10Kohm_0402 (CS31002FB26)

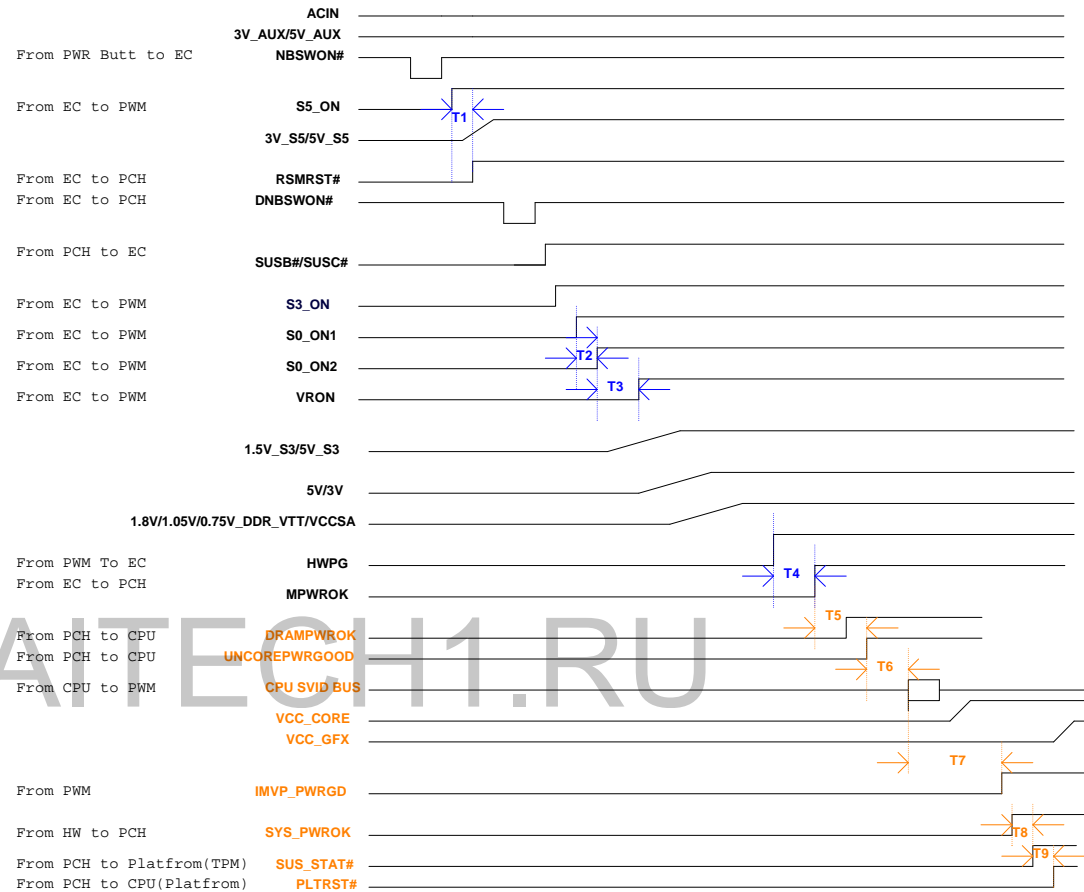
	N13P-GLP	N13P-LP
VR62	10Kohm_0402 (CS31002FB26)	NA

ID2	ID1	ID0	Model
0-R435	0-R438	0-R437	FJ8 UMA
0-R435	0-R438	1-R430	FJ8 Discrete
0-R435	1-R382	0-R437	PH6 UMA(Consumer)
0-R435	1-R382	1-R430	PH6 UMA(Commercial)
1-R384	0-R438	0-R437	PH6 N13P-LP
1-R384	0-R438	1-R430	PH6 N13P-GLP
1-R384	1-R382	0-R437	TBD
1-R384	1-R382	1-R430	TBD

B-29

		GLP 1GB HYN	GLP 1GB SAM	GLP 2GB HYN	GLP 2GB SAM	LP 2GB HYN	LP 2GB SAM
ROM_SCLK	VR44	NA	NA	NA	NA	CS24992FB26	CS24992FB26
	VR54	CS31502FB24	CS31502FB24	CS31502FB24	CS31502FB24	NA	NA
ROM_SI	VR41	NA	NA	NA	NA	CS24992FB26	CS24992FB26
	VR52	CS31502FB24	CS32002FB29	CS33012FB18	CS34532FB18	CS33012FB18	CS34532FB18
ROM_SO	VR43	NA	NA	NA	NA	CS31002FB26	CS31002FB26
	VR53	CS31002FB26	CS31002FB26	CS31002FB26	CS31002FB26	NA	NA
STRAP0	VR51	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18
	VR55	NA	NA	NA	NA	NA	NA
STRAP1	VR46	NA	NA	NA	NA	CS24992FB26	CS24992FB26
	VR56	CS34532FB18	CS34532FB18	CS34532FB18	CS34532FB18	CS24992FB26	CS24992FB26
STRAP2	VR47	CS24992FB26	CS24992FB26	CS24992FB26	CS24992FB26	NA	NA
	VR57	NA	NA	NA	NA	CS32002FB29	CS32002FB29
STRAP3	VR48	NA	NA	NA	NA	CS24992FB26	CS24992FB26
	VR58	CS24992FB26	CS24992FB26	CS24992FB26	CS24992FB26	NA	NA
STRAP4	VR50	NA	NA	NA	NA	CS34532FB18	CS34532FB18
	VR59	NA	NA	NA	NA	NA	NA

System Power-ON Sequence



System Power Sequence

EC Control:

T1: S5_ON TO RSMRST# = 20ms (spec:mini 10ms)

T2: S0_ON1 TO S0_ON2 = 500us

T3: S0_ON2 TO VRON = 10ms

T4: HWPG TO MPWROK = 110ms (spec:mini 99ms)

Note:HWPG NEED TO BE HIGH at that time

System:

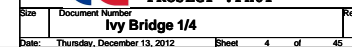
T5: MPWROK to UNCOREPWROK =2ms(Min)

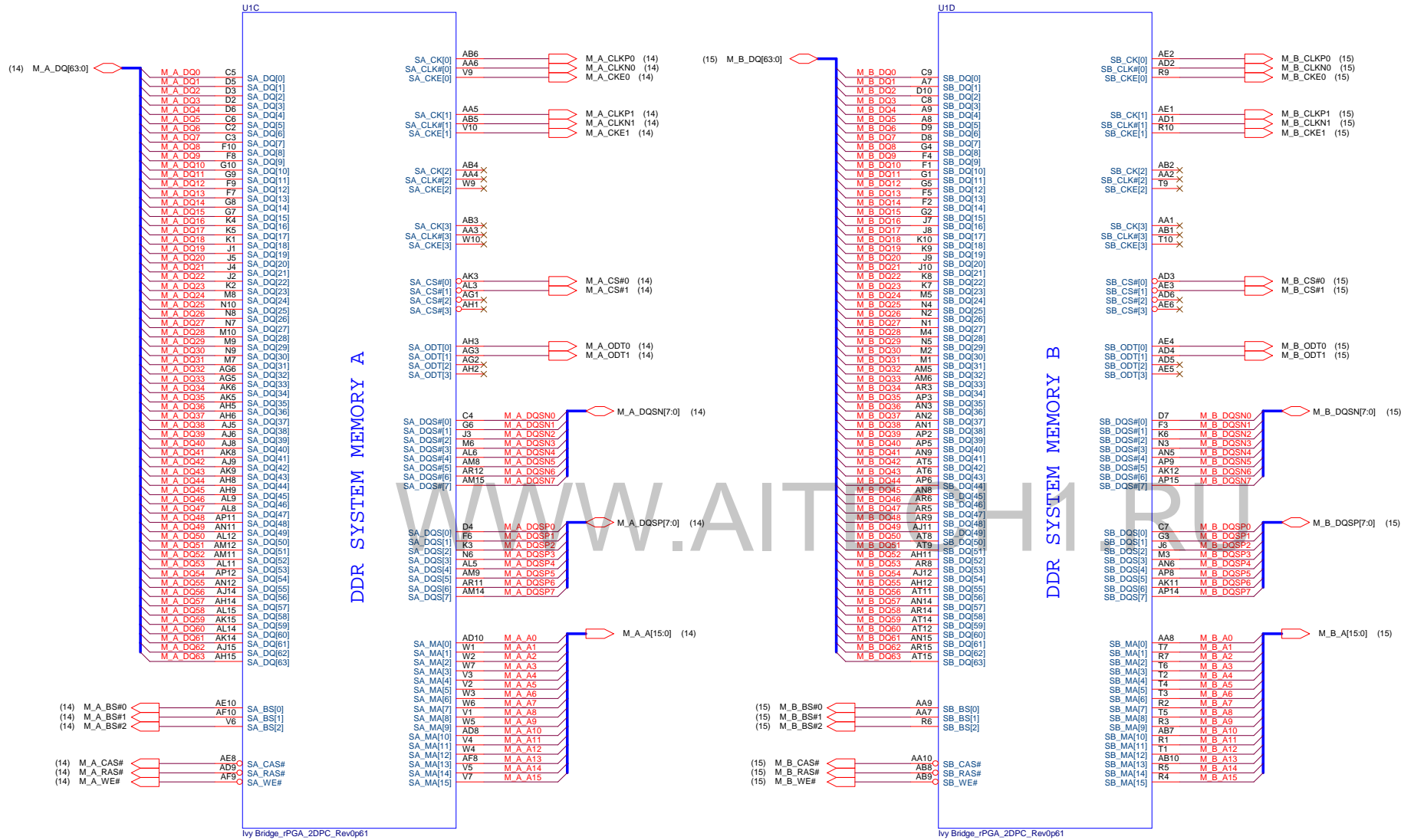
T6: UNCOREPWROK to SVID Packet =500us(Max)

T7: SVID Packet to IMVP_PWRGD =5ms(Max)

T8: SYS_PWROK to SUS_STAT# =1ms(Min)

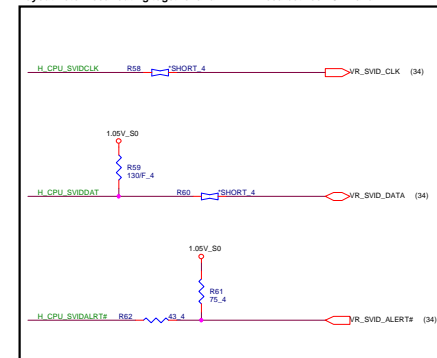
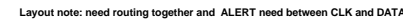
T9:SUS_STAT# to PLTRST# =60us(Min)





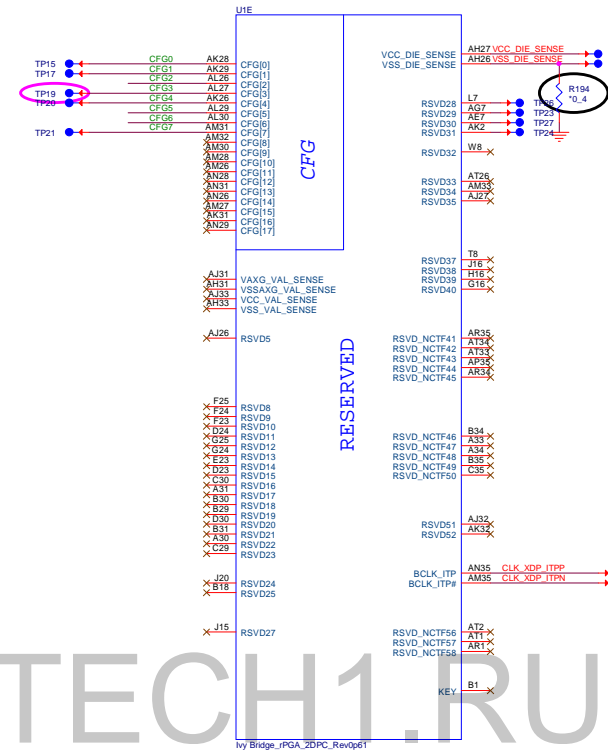
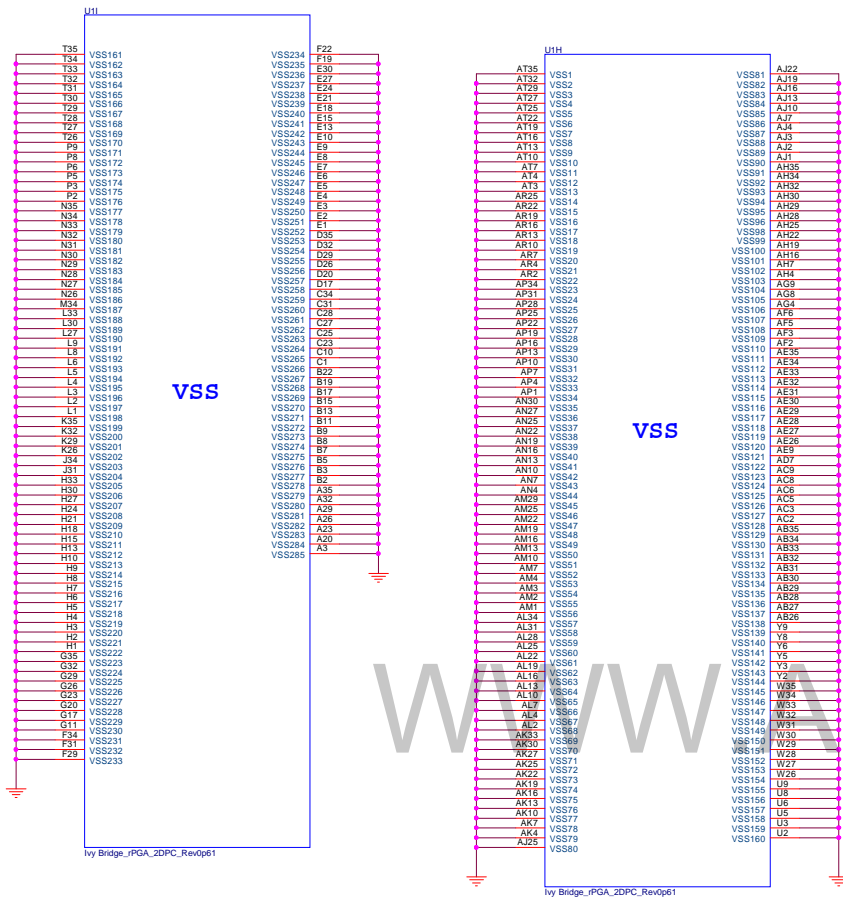
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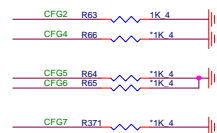
Ivy Bridge Processor (GND)

Ivy Bridge Processor (RESERVED, CFG)

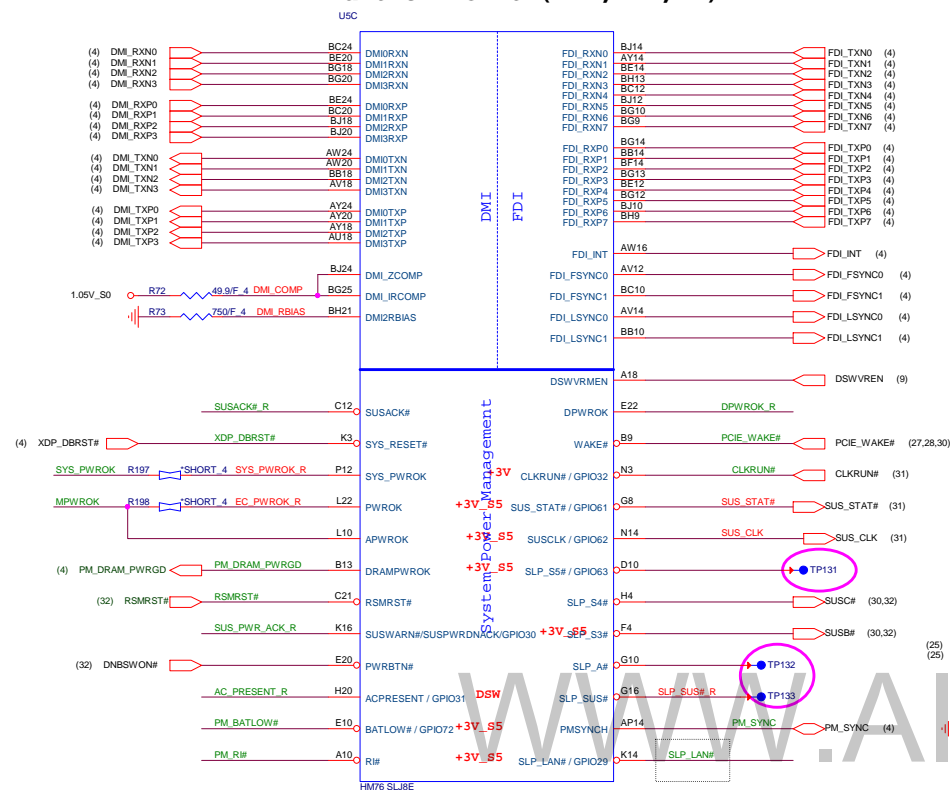


Processor Strapping

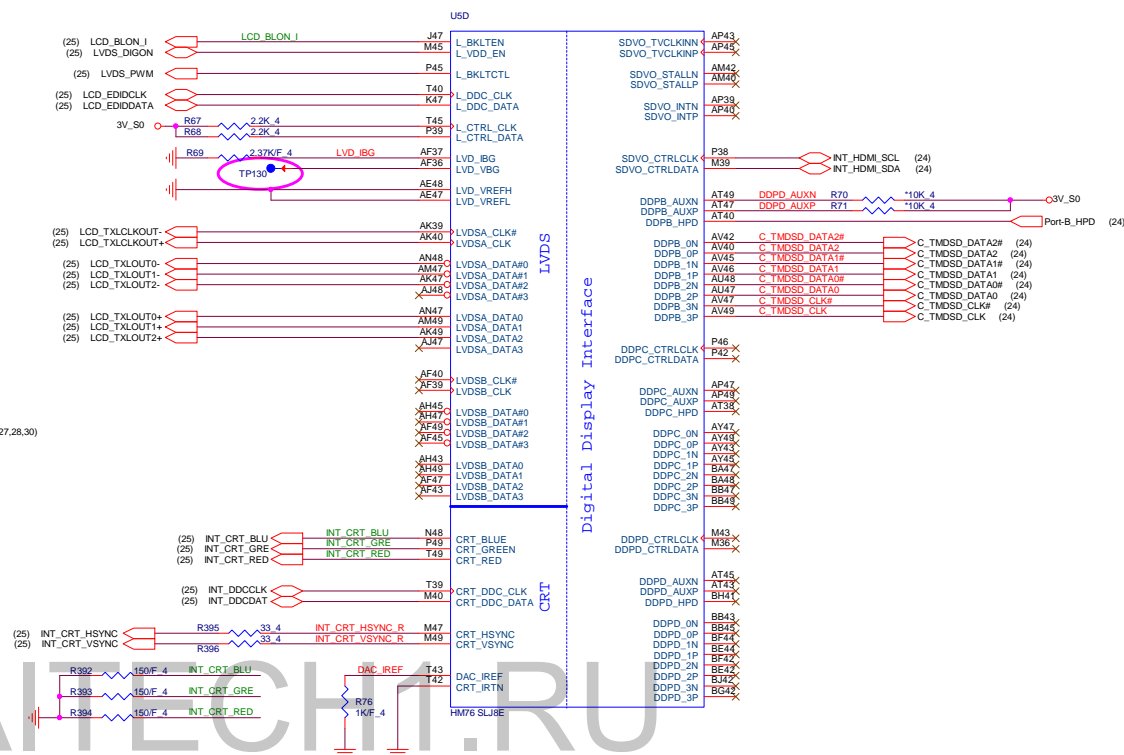
CFG2	0	PCIe X16 LANE Reversed
	1	Normal Operation
CFG3	0	PCIe X4 LANE Reversed
	1	Normal Operation
CFG4	0	Enable; An ext DP device is connected to eDP
	1	Disable; No physical DP attached to eDP
CFG(5:6)	00	1 x 8 , 2 x 4 PCIe
	01	Reserve
	10	2 x 8 PCIe
	11	1 x 16 PCIe
CFG7	0	PEG Wait for BIOS for training
	1	PEG Train immediately following PLT_RST#



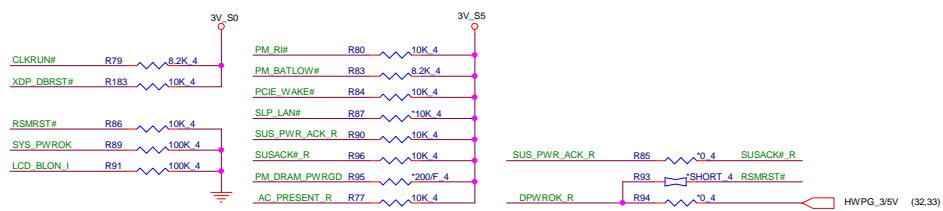
Panther Point (DMI,FDI,PM)



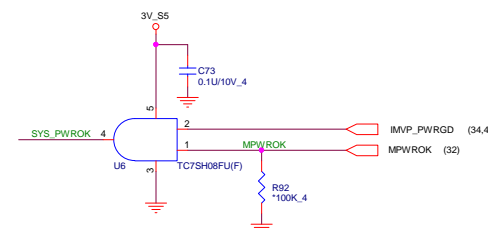
Panther Point (LVDS,DDI)



PCH Pull-high/low



System PWR_OK



[illegible]

Signal Name	Resistor Value	Resistor Label	ACZ Pin
(29) BIT_CLK_AUDIO	33.4	R115	ACZ_BITCLK
(29) ACZ_SYNC_AUDIO	33.4	R117	ACZ_SYNC_R
(29) ACZ_RST#_AUDIO	33.4	R118	ACZ_RST#
(29) ACZ_SDOUT_AUDIO	33.4	R120	ACZ_SDOUT
(29) ACZ_SDINO_AUDIO	-	-	ACZ_SDINO_AUDIOIO

3V_S5

R152 210F_4

R123 210F_4

R124 210F_4

PCH_JTAG TMS

PCH_JTAG TDI

PCH_JTAG TDO

PCH_JTAG TCK

R126 51_4

R153 100F_4

R127 100F_4

R128 100F_4

Ground

C-39

PC#_SPI_CS0# 1
PC#_SPI_CLK# 2
PC#_SPI_SI 3
PC#_SPI_SO 4

R557 33.4
R461 33.4
R462 33.4
R463 33.4

PC#_SPI_CS0 R# 1
PC#_SPI_CLK# R 2
PC#_SPI_SI R 3
PC#_SPI_SO R 4

U7
CE# VDD 8
SCK 6
SI 5
SO HOLD# 7
WP# VSS 4

W25016CVSSIG

3V_S0 0.1uF/10V C82
3.3kF/4 R141
22p50V_4N C81

4MB BIOS

C-39

PC#_SPI_CS1# 1
PC#_SPI_CLK# 2
PC#_SPI_SI 3
PC#_SPI_SO 4

R459 33.4
R472 33.4
R463 33.4
R484 33.4

PC#_SPI_CS1 R# 1
PC#_SPI_CLK# R 2
PC#_SPI_SI R 3
PC#_SPI_SO R 4

U35
CE# VDD 8
SCK SI 6
SO HOLD# 7
WP# VSS 4

W25026BVSSIG

3V_S0 0.1uF/10V C230
3.3kF/4 R228
22p50V_4N C229

[illegible]

Pin Name	Strap description	Sampled	Configuration										
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	3V_S0 ○ R121 ~1K 4 PCBEEP									
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	R122 ~1K 4 PCI_GNT3# (10)									
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	3V_RTC ○ R125 ~330K 4 PCH_INVRMEN									
GNT1# / GPIO51	Boot BIOS Selection 1 [bit-1]	PWROK	<table border="1"> <thead> <tr> <th>GNT1#</th><th>GPIO19</th><th>Boot Location</th></tr> </thead> <tbody> <tr> <td>1</td><td>1</td><td>SPI</td></tr> <tr> <td>0</td><td>0</td><td>LPC</td></tr> </tbody> </table>	GNT1#	GPIO19	Boot Location	1	1	SPI	0	0	LPC	R129 ~1K 4 GNT1# (10) R130 ~1K 4 GPIO19
GNT1#	GPIO19	Boot Location											
1	1	SPI											
0	0	LPC											
GPIO19	Boot BIOS Selection 0 [bit-0]	PWROK											
HDA_SDO	Flash Descriptor Security	RSMRST	1 = Override 0 = Default (weak PD 20K)	3V_S0 ○ R131 ~1K 4 ACZ_SDOUT ACZ_SDOUT (32)									
DF_TVS	DMI/FDI Termination voltage	PWROK	0 = Set to Vss 1 = Set to Vcc (weak pull-down 20K)	R132 ~2.2K 4 1.8V_S0 DF_TVS (11) R133 ~1K 4 H_SMB_IVSM#									
GPIO28	On-die PLL Voltage Regulator	RSMRST#	0 = Disable 1 = Enable (Default)	3V_AUX ○ R134 ~10K 4 PLL_ODVR_EN (11) R135 ~1K 4									
HDA_SYNC	On-Die PLL VR Voltage Select	RSMRST	0 = Support by 1.8V (weak pull-down) 1 = Support by 1.5V	3V_S5 ○ R136 ~1K 4 ACZ_SYNC									
GPIO15	TLS Confidentiality	RSMRST	0 = Default, TLS no Confidentiality 1 = TLS Confidentiality	3V_S5 ○ R137 ~1K 4 GPIO15 (11)									
DSWVRMEN	Deep S4/S5 Well On -Die Voltage Regulator Enable	ALWAYS	0 = Disable 1 = Enable	3V_RTC ○ R139 ~330K 4 DSWVREN (8) R140 ~330K 4									
INIT3_3V#	Reserved	PWROK	1 = Default (weak pull-up 20K)	Should not pull low. leave as No Connect									
GNT2# / GPIO53	ESI Strap (Server Only)	PWROK	1 = Default. Should not be pulled low for desktop and mobile	Should not pull low for desktop and mobile									
L_DDC_DATA	LVDS Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V									
SDVO_CTRLDATA	Port B Detected	PWROK	0 = Default. Not Detected 1 = Detected	1 = PU to 3V									
DDPC_CTRLDATA	Port C Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
DDPD_CTRLDATA	Port D Detected	PWROK	0 = Default. Not Detected 1 = Detected	0=NC									
SATA3GP / GPIO37	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									
SATA2GP / GPIO36	Reserved	PWROK	0 = Default	Should not be pulled high when strap is sampled									

NEW CARD



Panther Point-M (PCI-E,SMBUS,CLK)



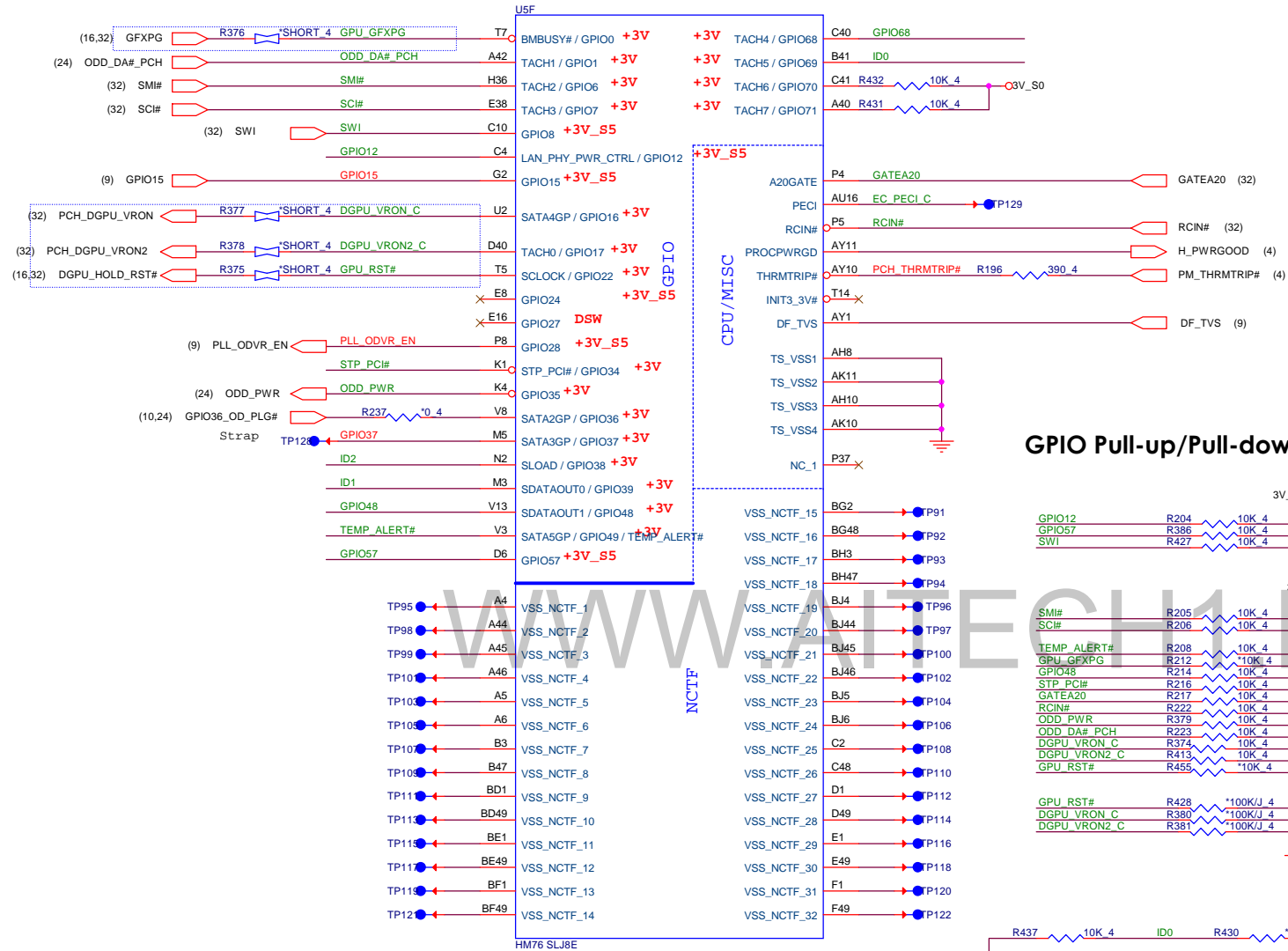
PCI/USBOC# PU



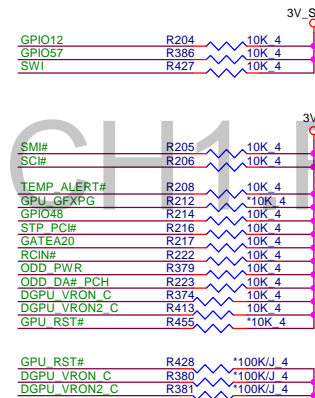
SMBUS Level Shift



Panther Point (GPIO,VSS_NCTF,RSVD)

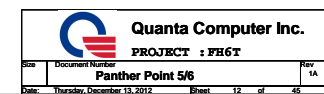


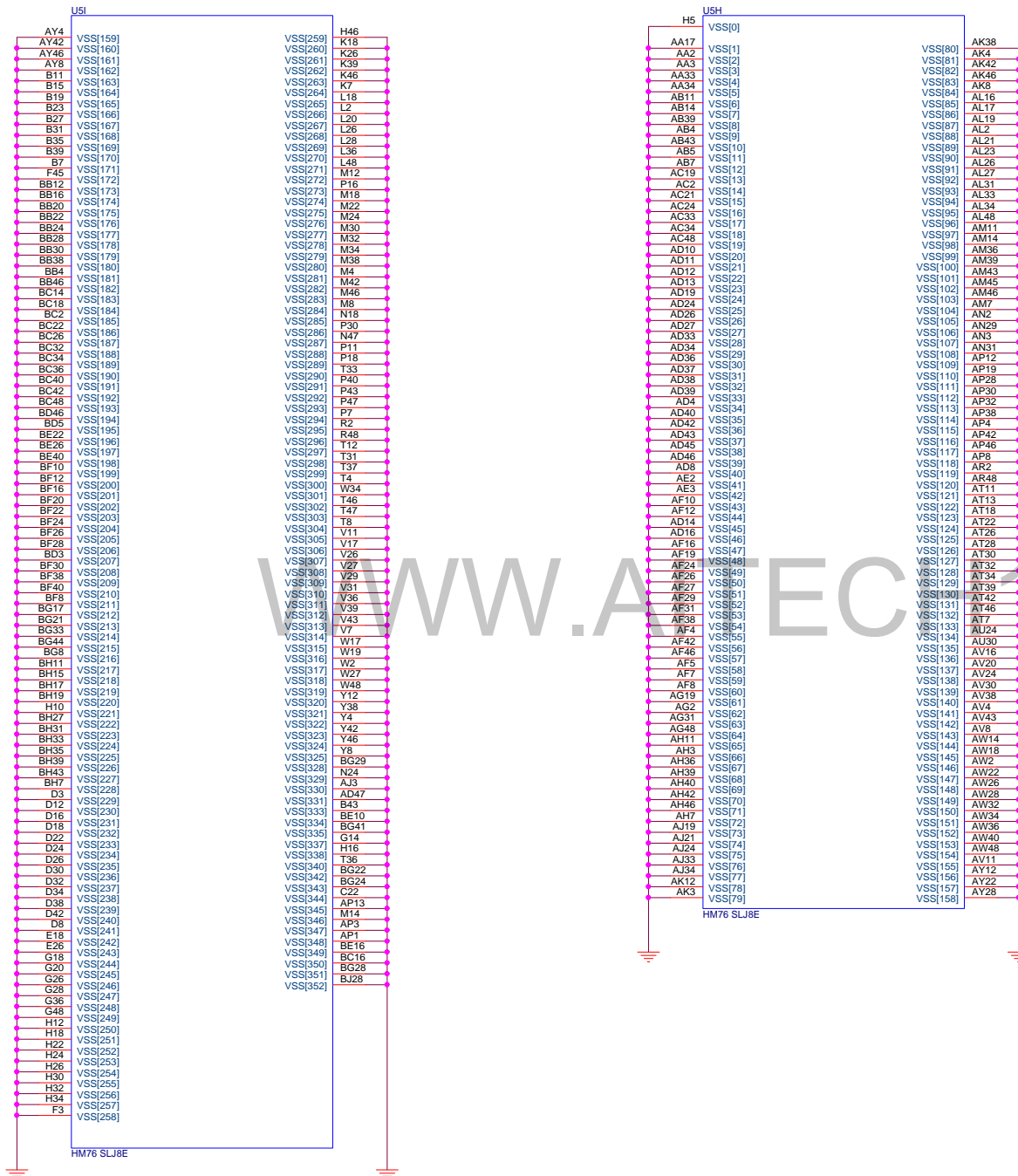
GPIO Pull-up/Pull-down



GPIO68	ID2	ID1	ID0	Model
1	0	0	0	FH6B UMA with click pad
1	0	0	1	
1	0	1	0	FH6 UMA(Consumer)
1	0	1	1	FH6 UMA(Commercial)
1	1	0	0	FH6 N13P-LP
1	1	0	1	FH6 N13P-GLP
1	1	1	0	TBD
1	1	1	1	TBD
0	0	1	0	FH6T UMA
0				
0				

Panther Point-M (POWER)



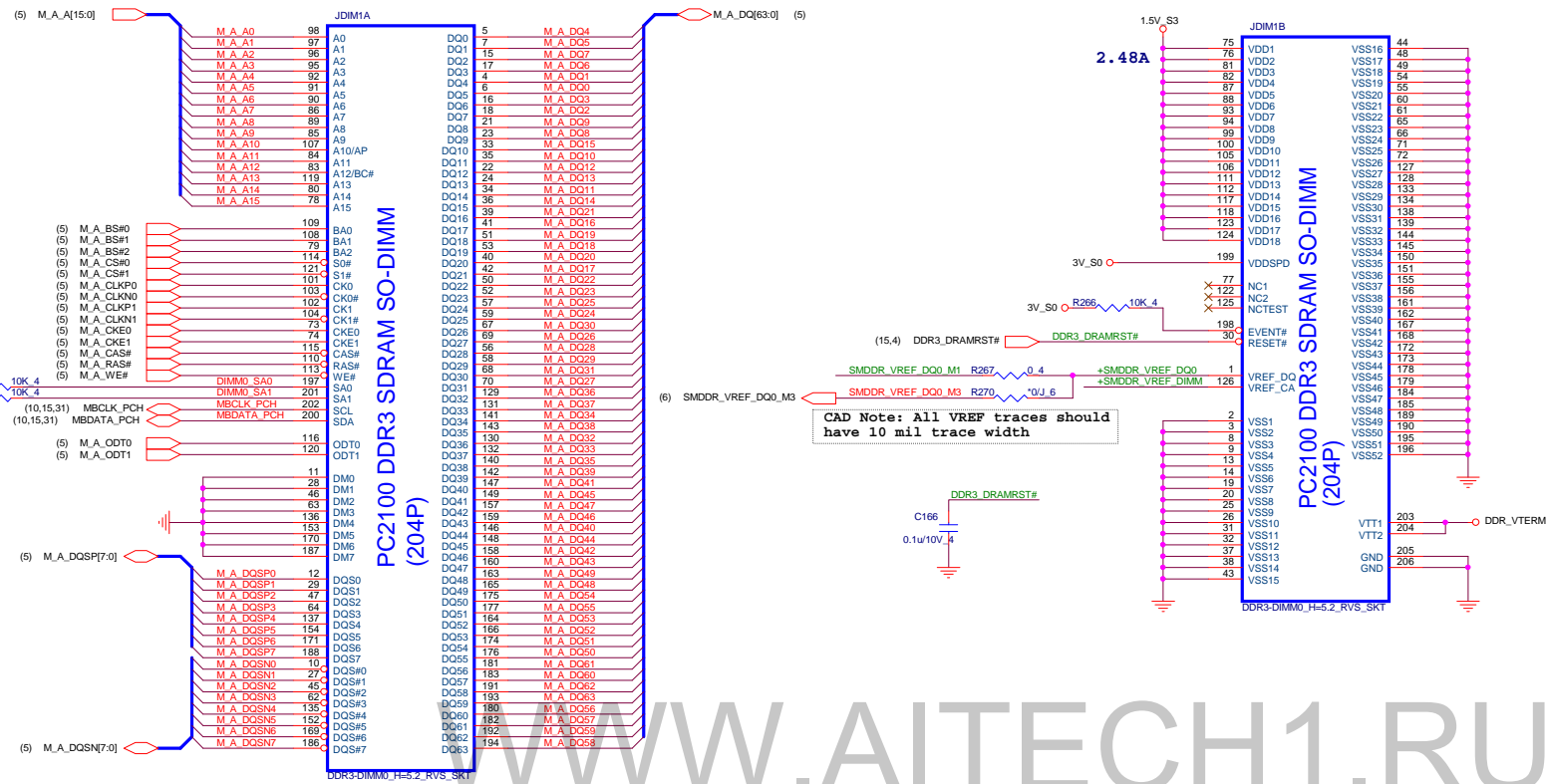


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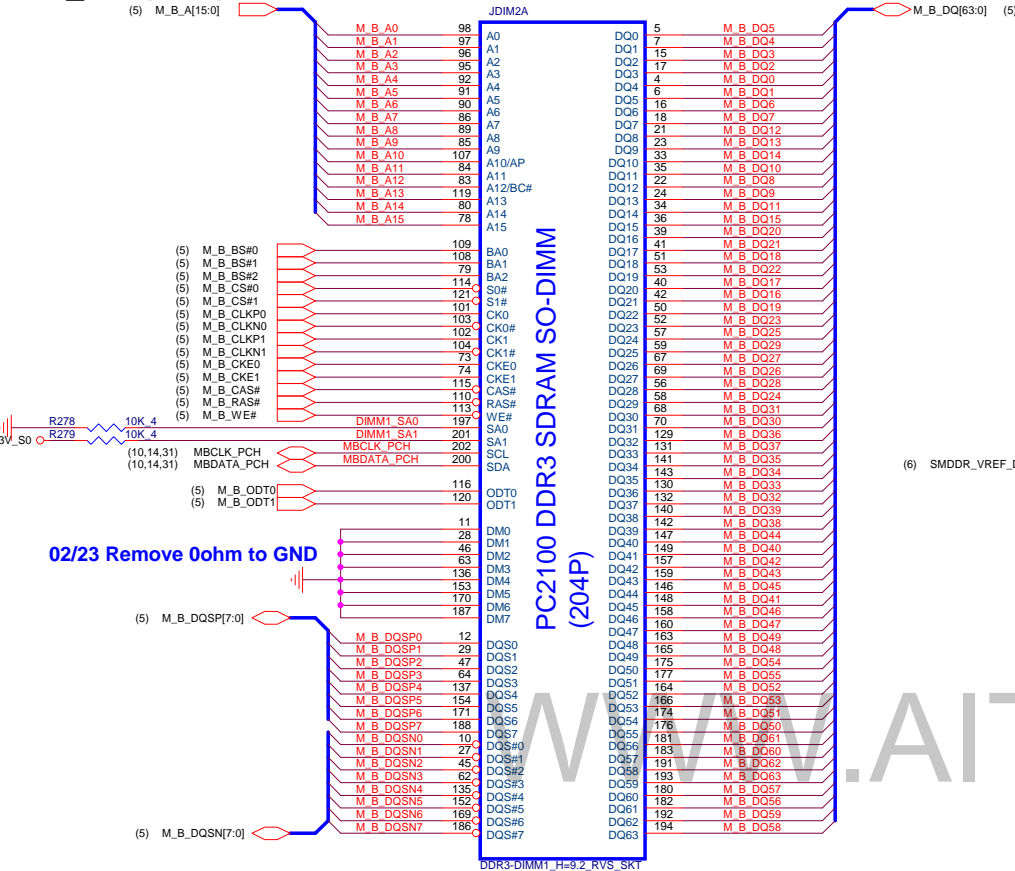
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	Panther Point 6/6	1A
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DDR_STD (DDR)



DDR_RVS (DDR)

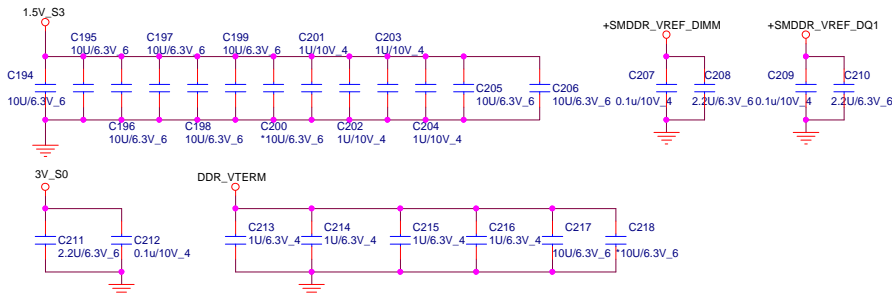


02/23 Remove 0ohm to GND

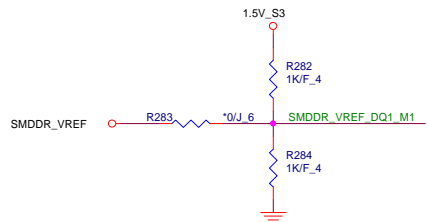
PC2100 DDR3 SDRAM SO-DIMM (204P)

DDR3-DIMM1_H=9.2_RVS_SK1

Place these Caps near So-Dimm1.

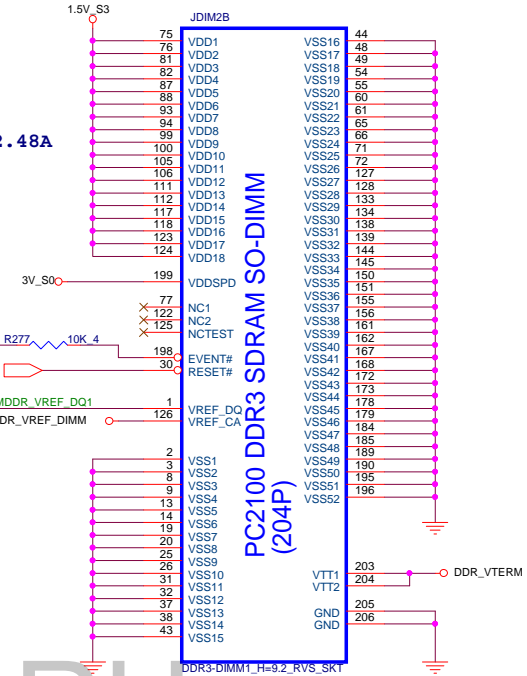


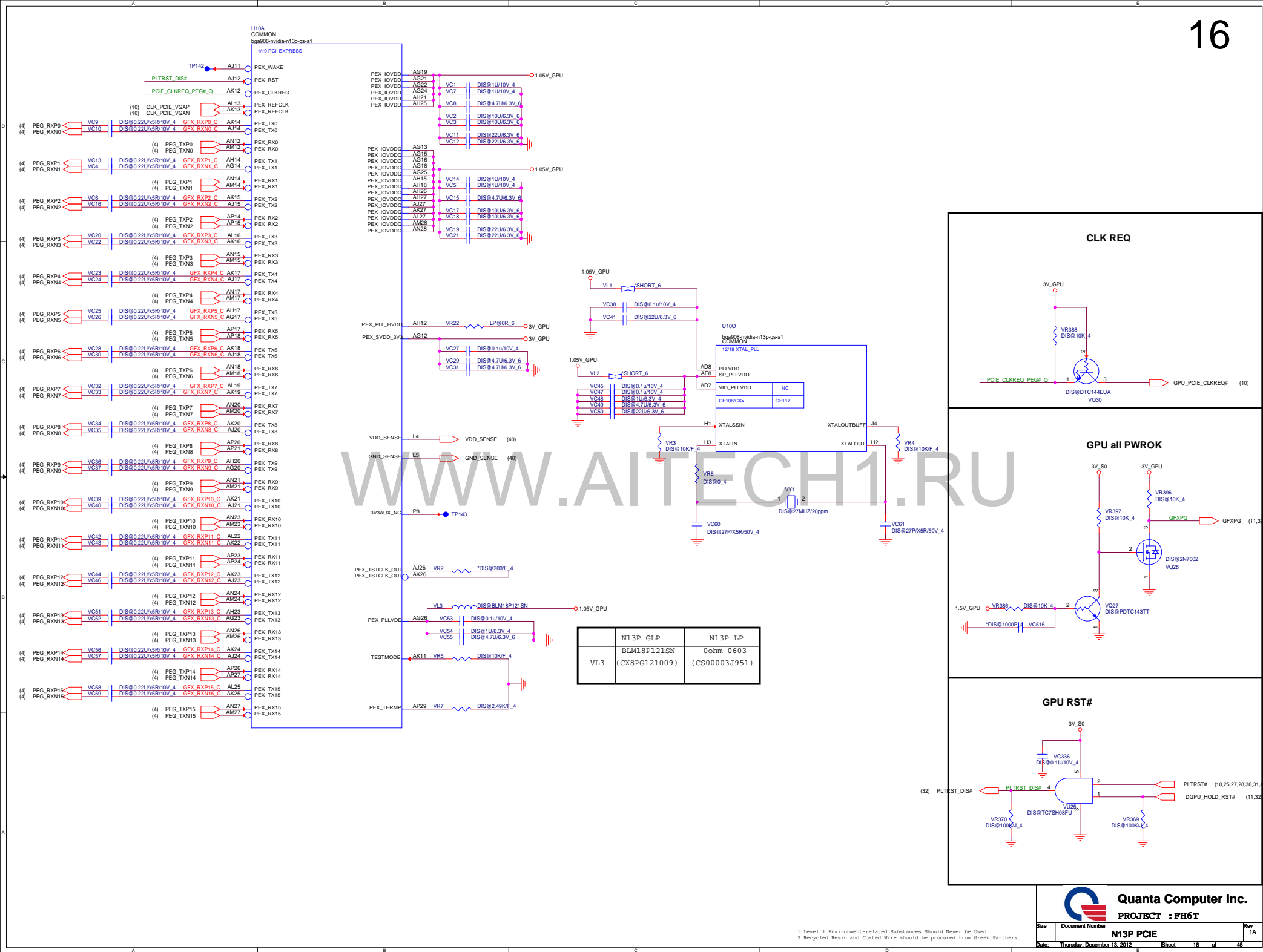
VREF DQ1 M1 Solution

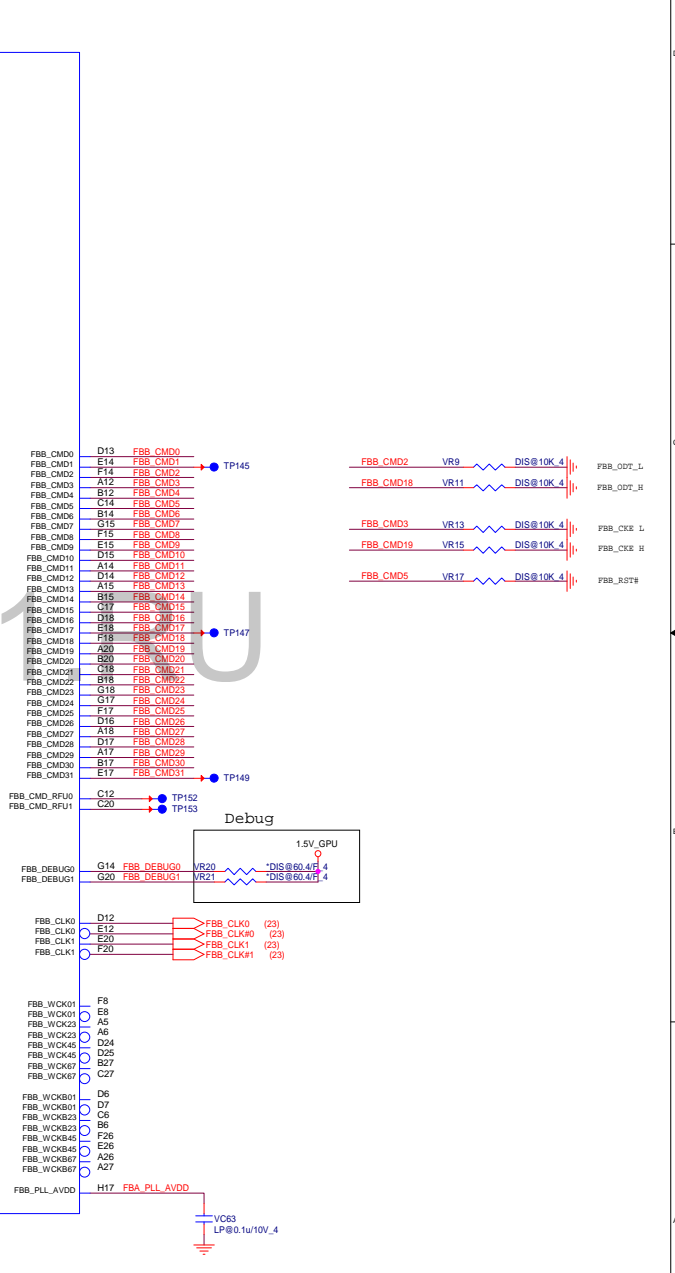
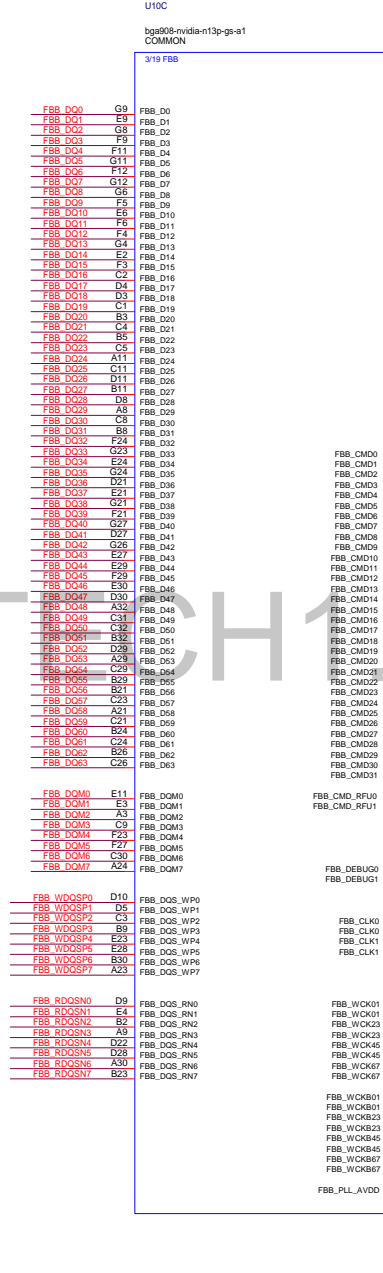


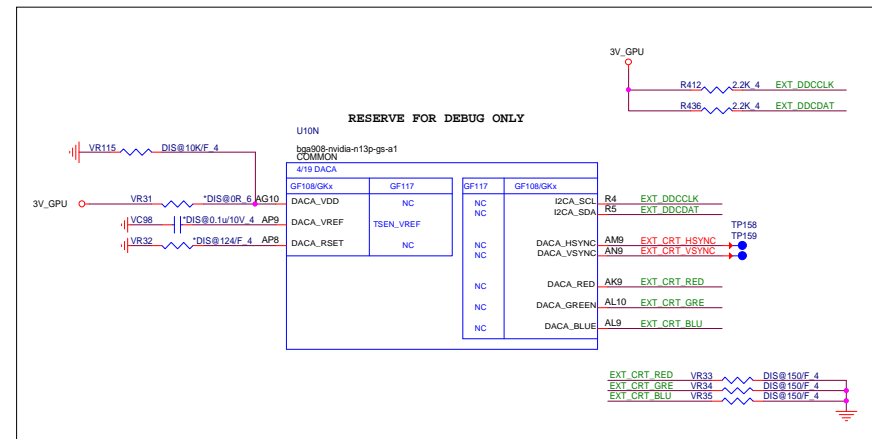
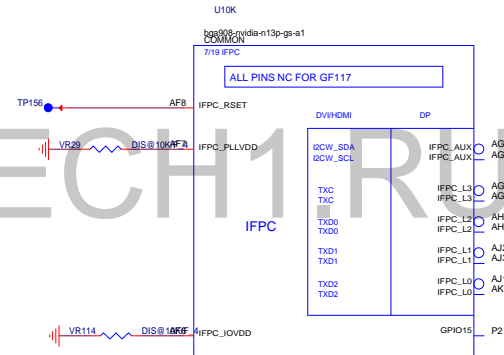
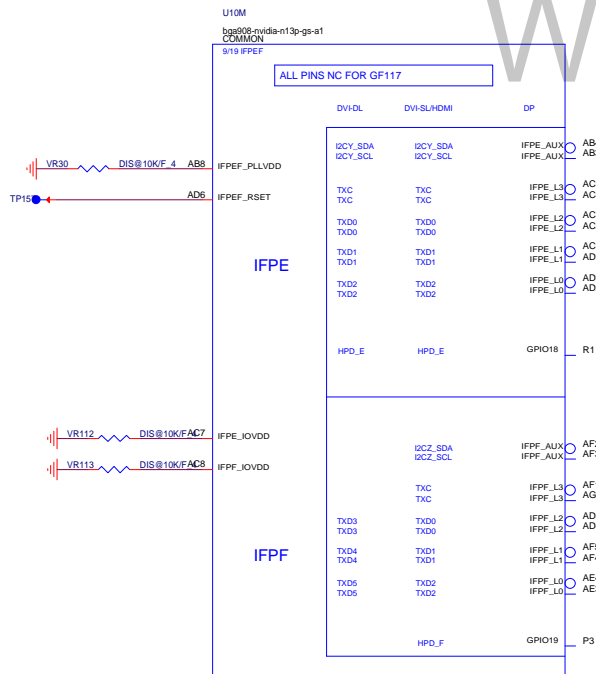
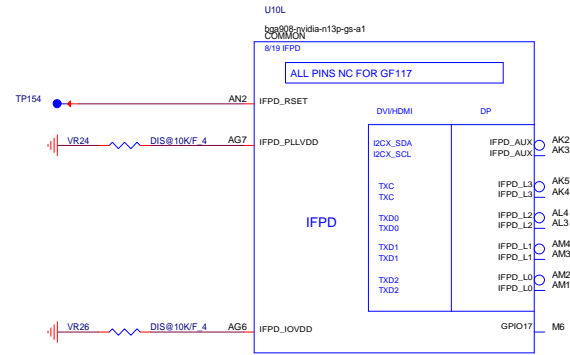
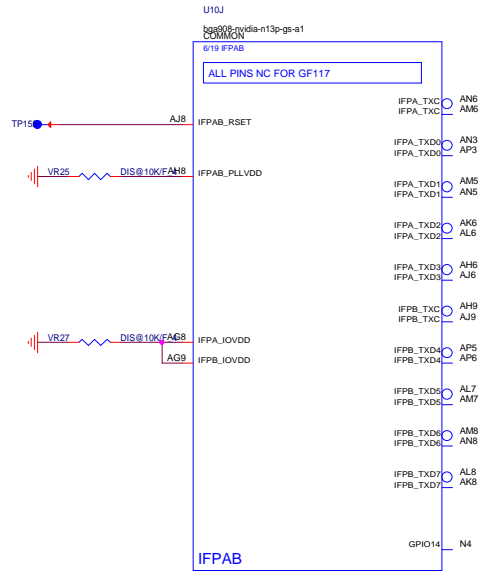
2.48A

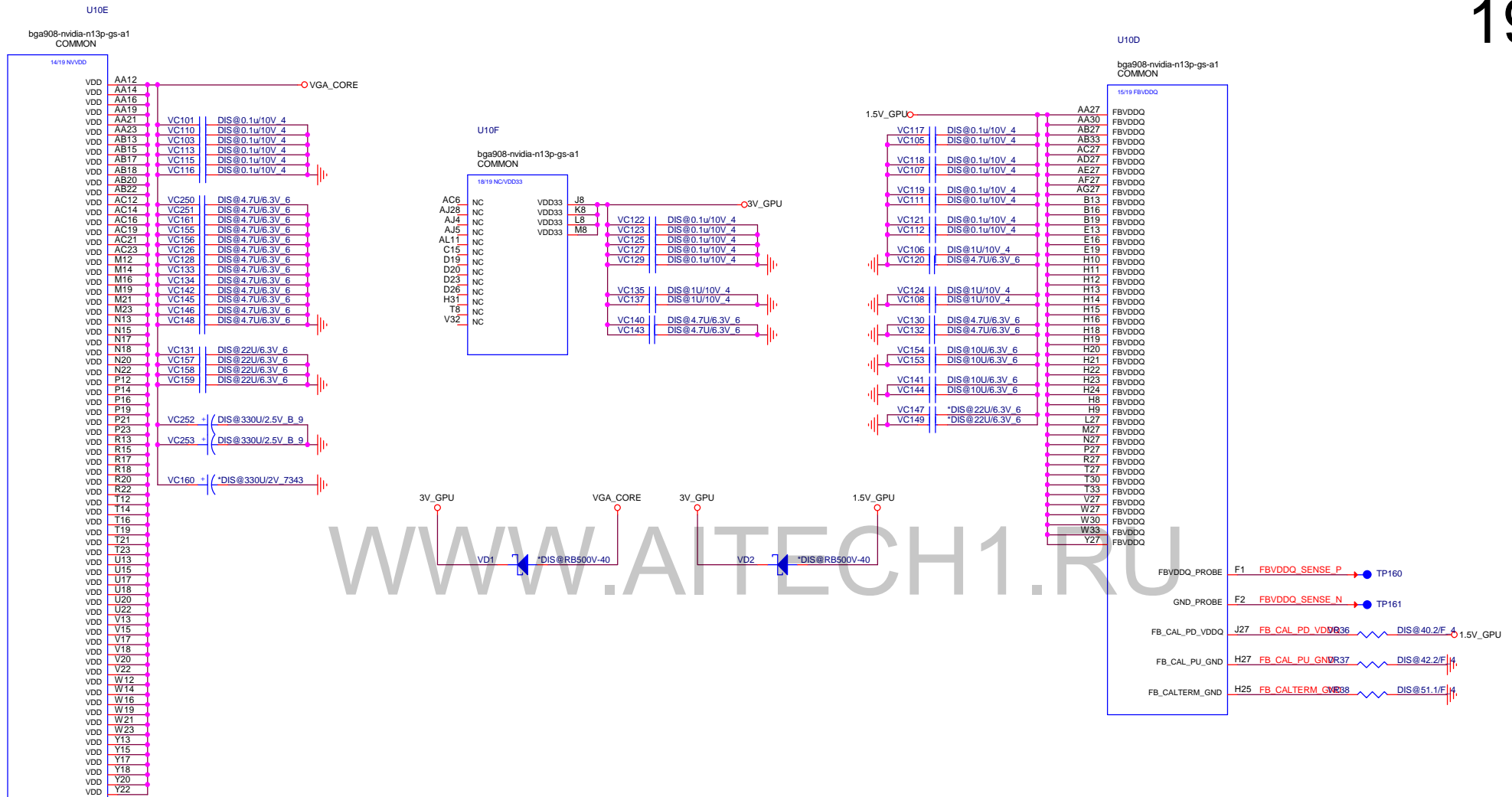
CAD Note: All VREF traces should have 10 mil trace width







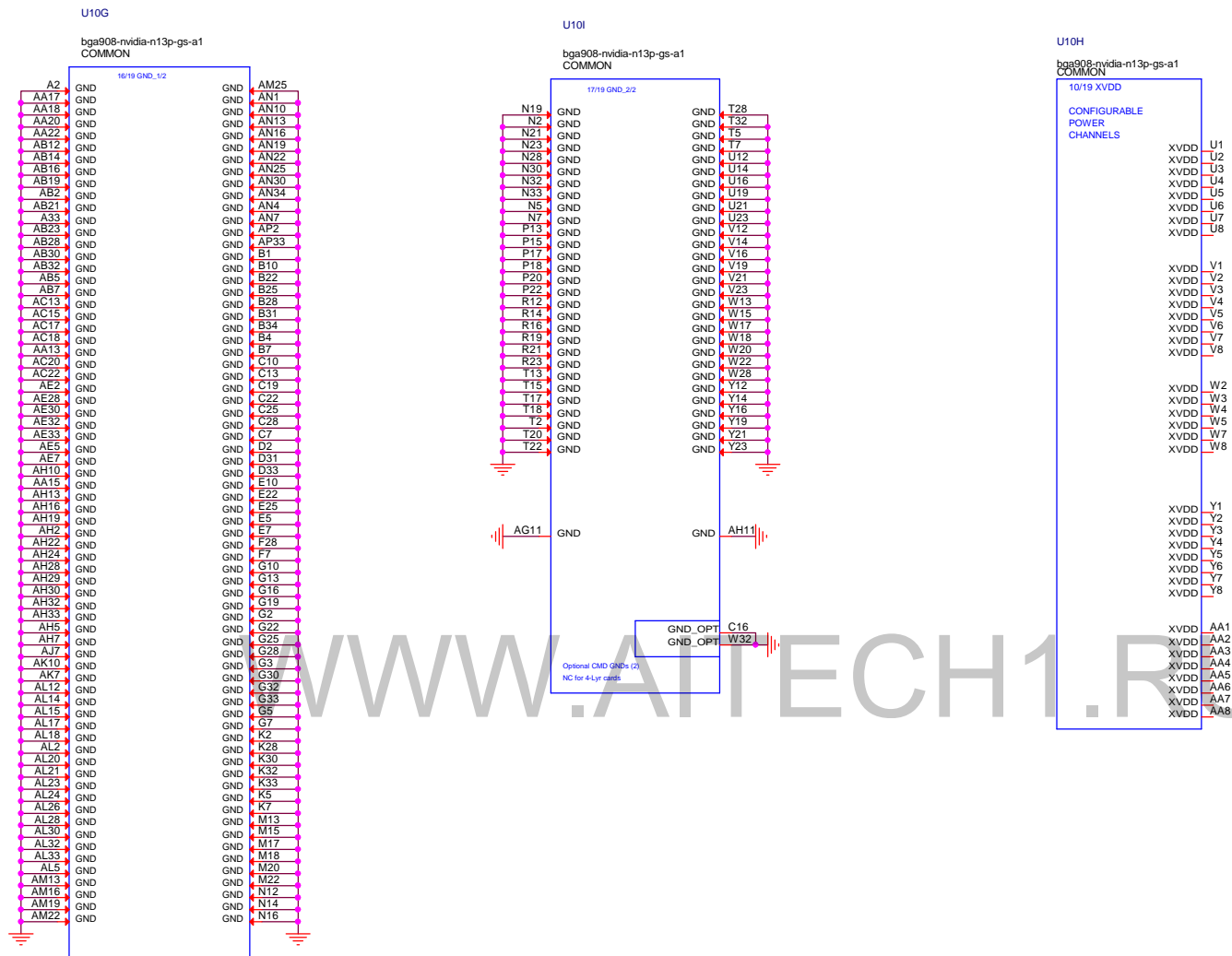




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	N13P POWER	1A
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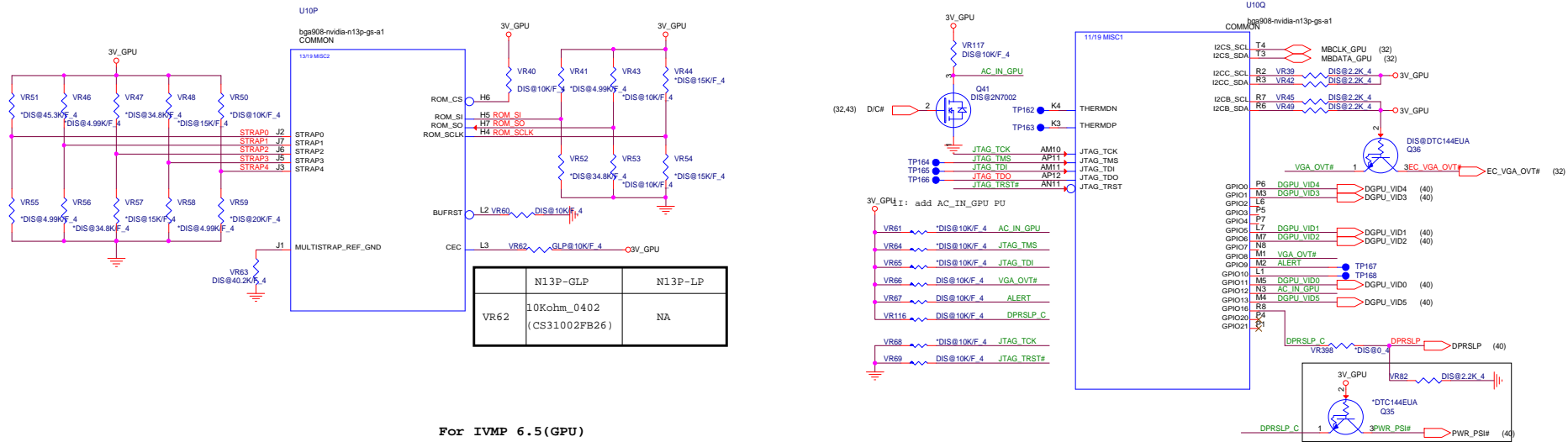


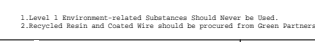
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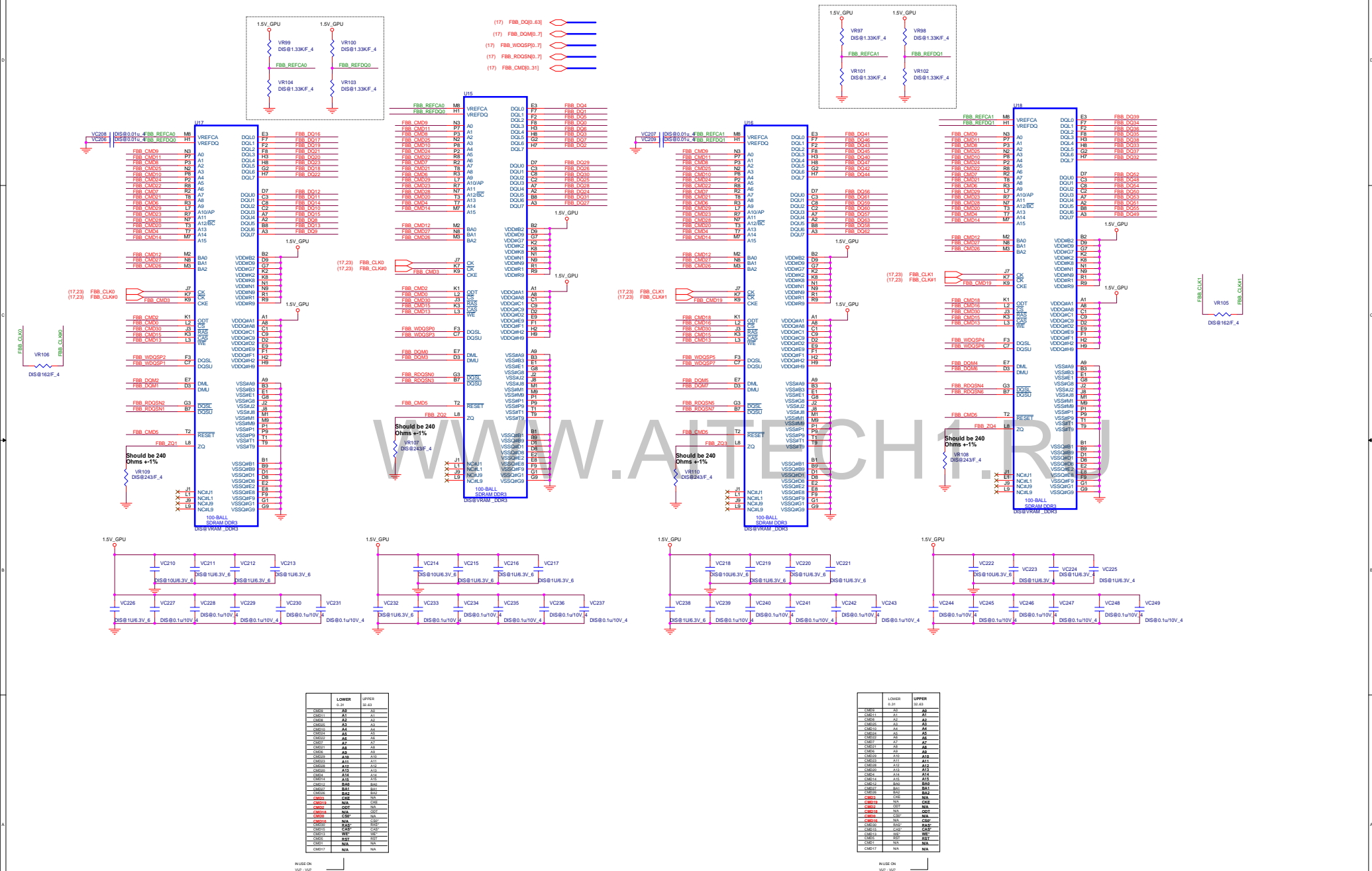
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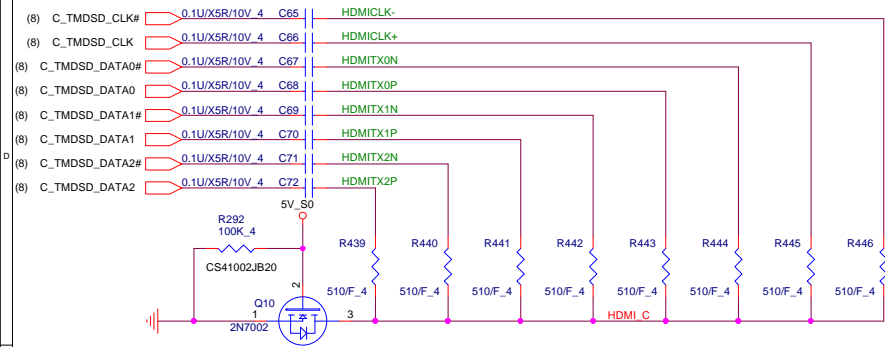
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	N13P GND	1A
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1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.

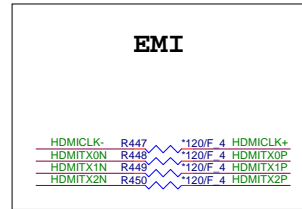
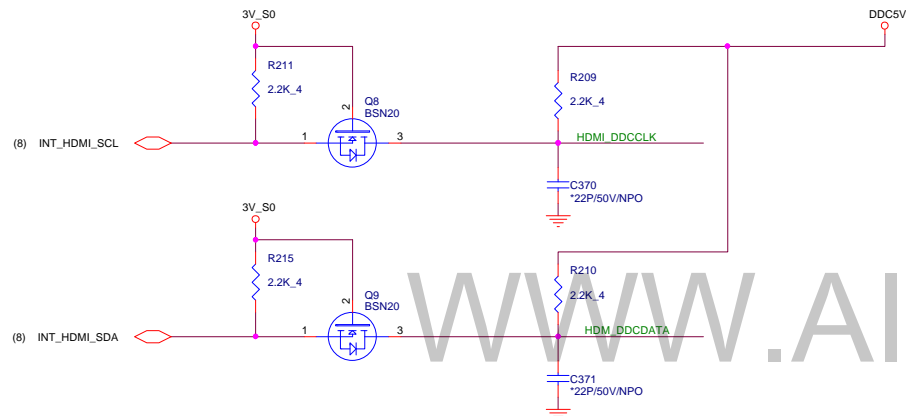






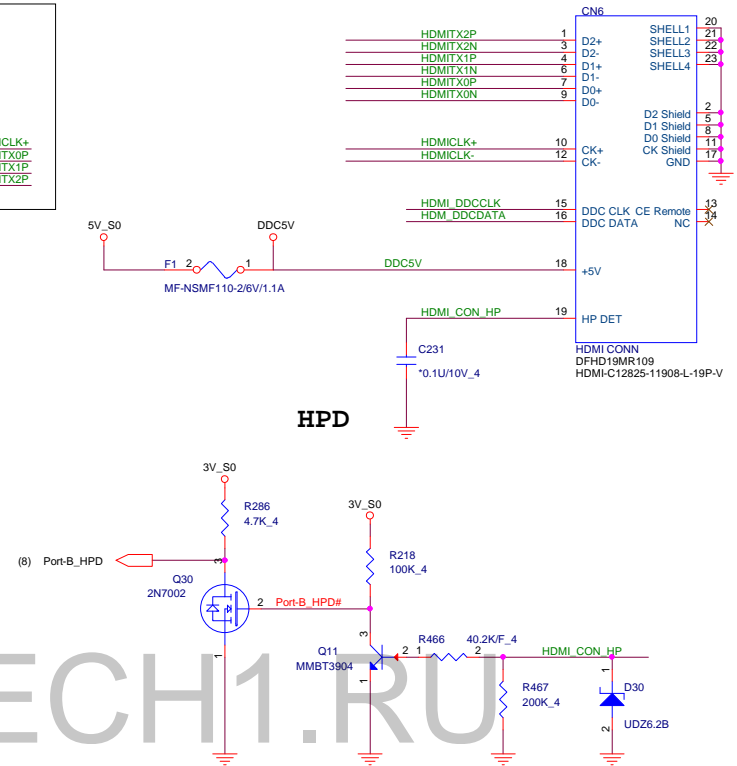


DDC Level Shift



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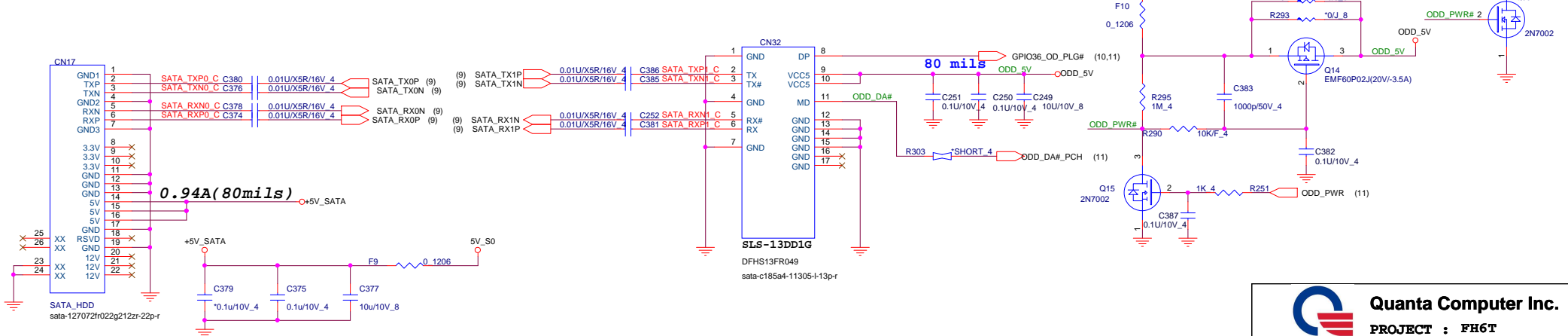
HDMI Conn



HPD

SATA ODD

2.5" SATA HDD



40mils

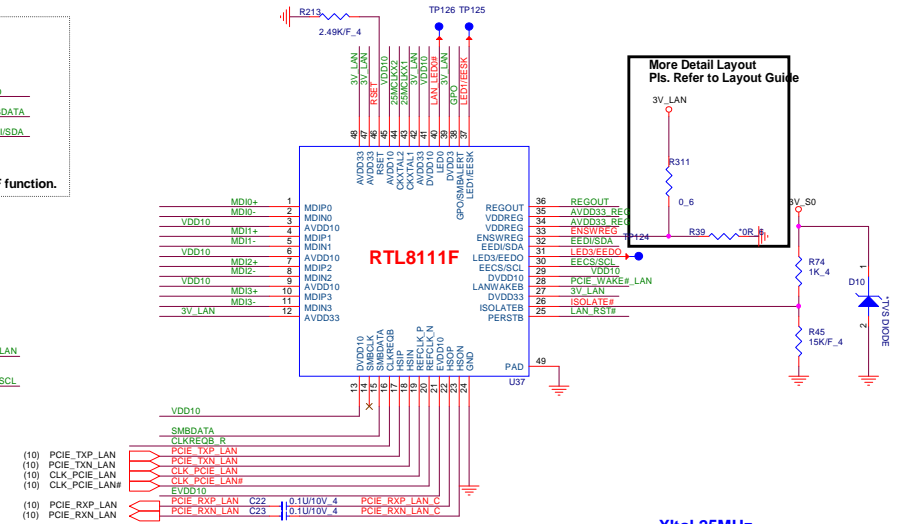
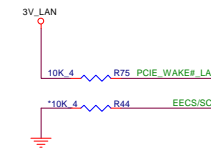
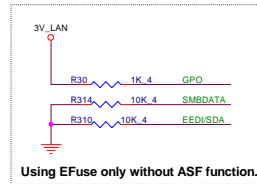
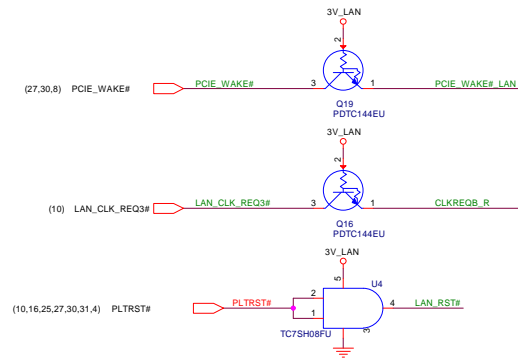


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USB 3.0 CONN

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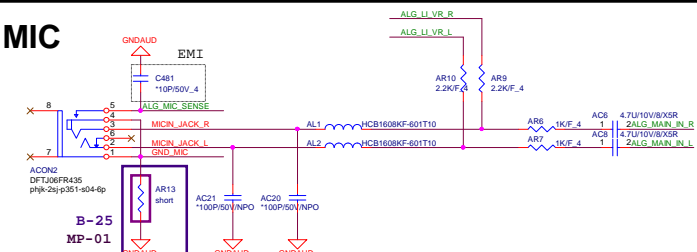
CBO	CB1	Status
0	0	Auto Dection Charge Mode
0	1	Force Dedicated Charger Mode
1	0	Pass Through Mode
1	1	Pass Through Mode with CDP or SDP(SIG55584 only)



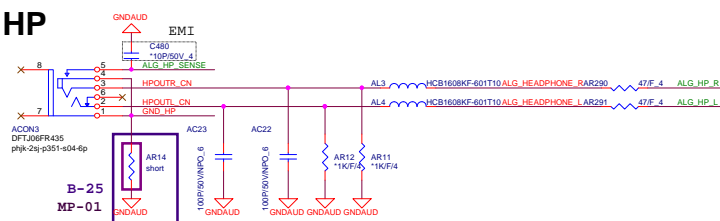
More Detail Layout
Pls. Refer to Layout Guide

X'tal 25MHz</

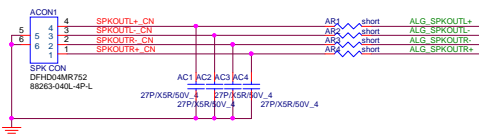
MIC



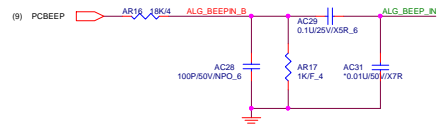
HP



SPKR



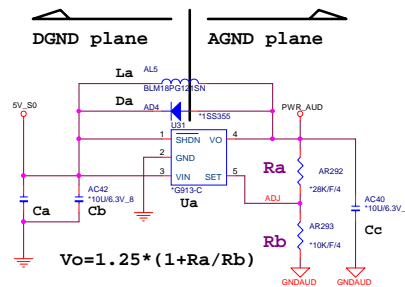
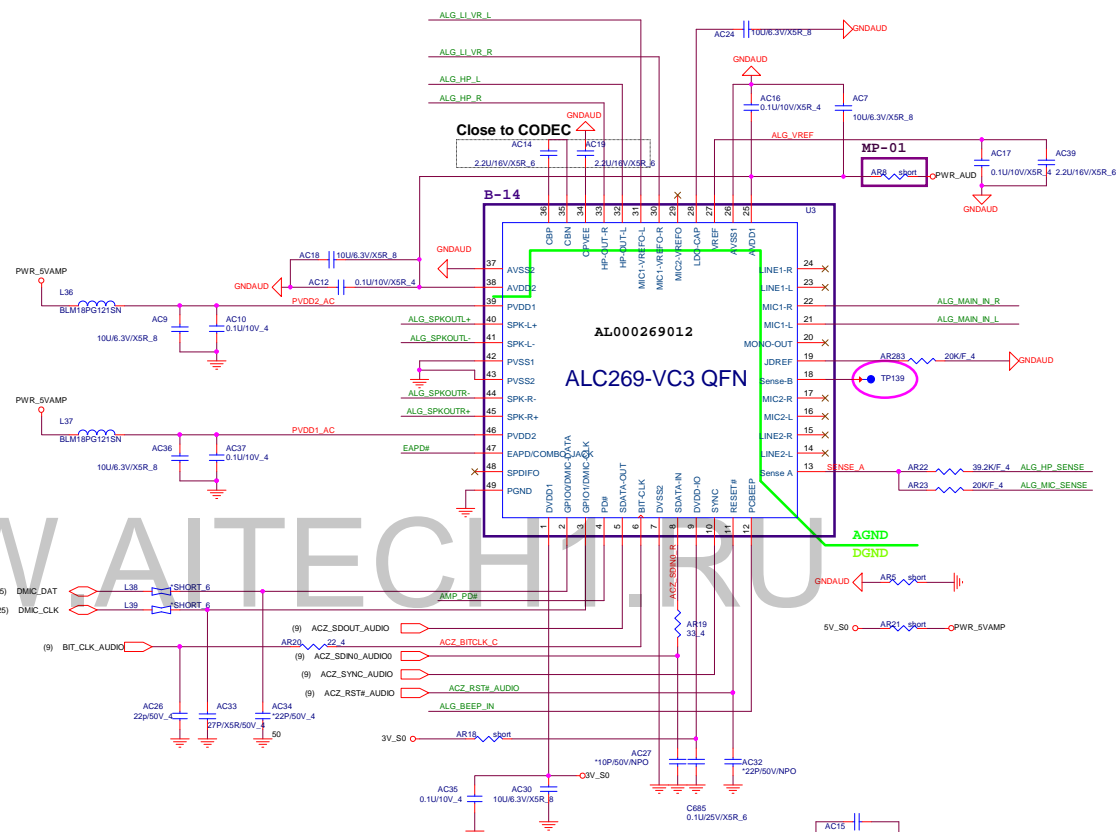
BEEP

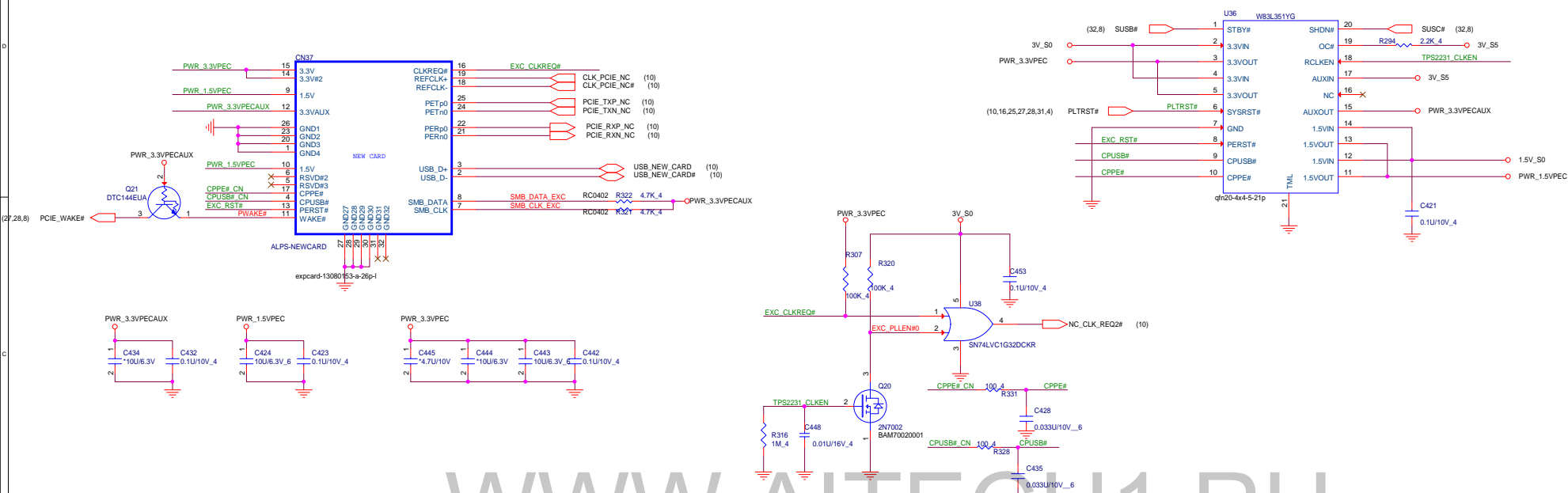


VOLMUTE

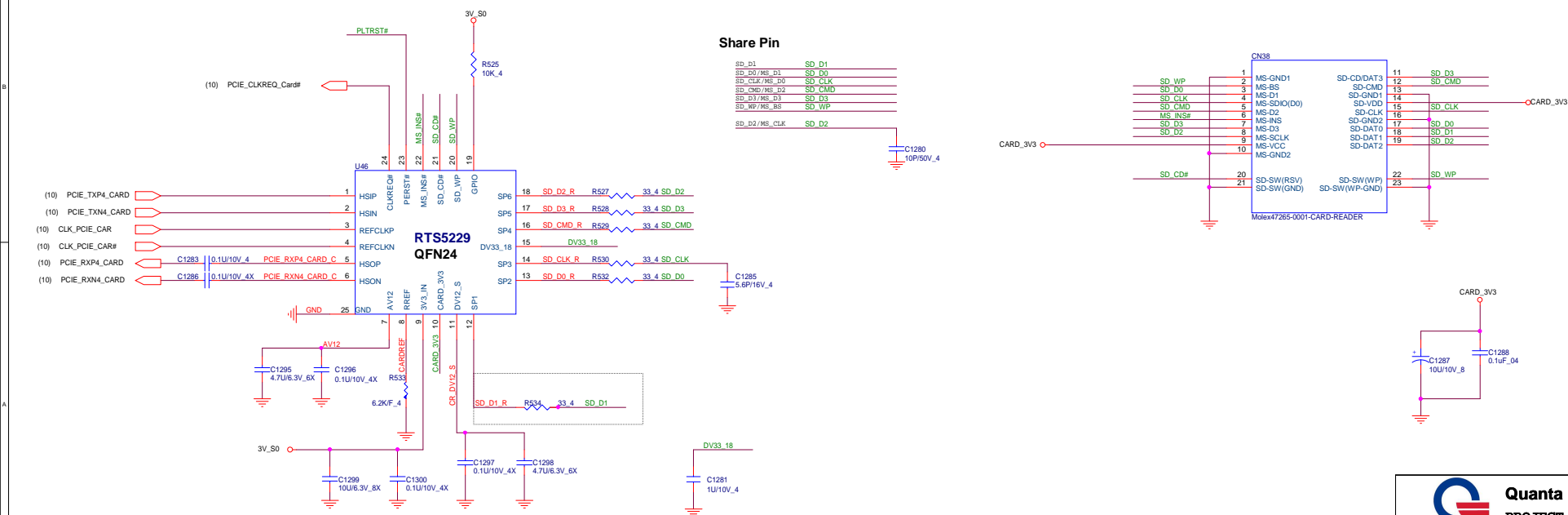


Codec ALC269-VC3

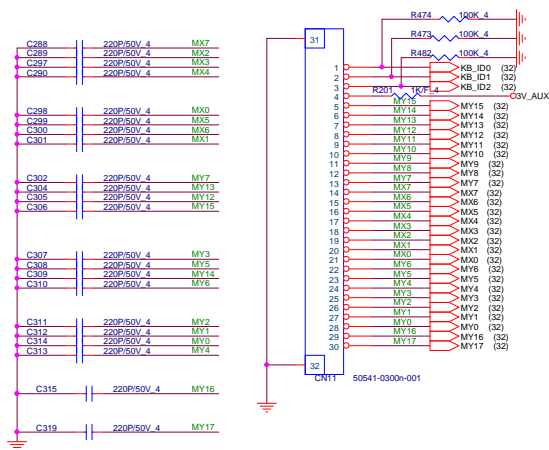




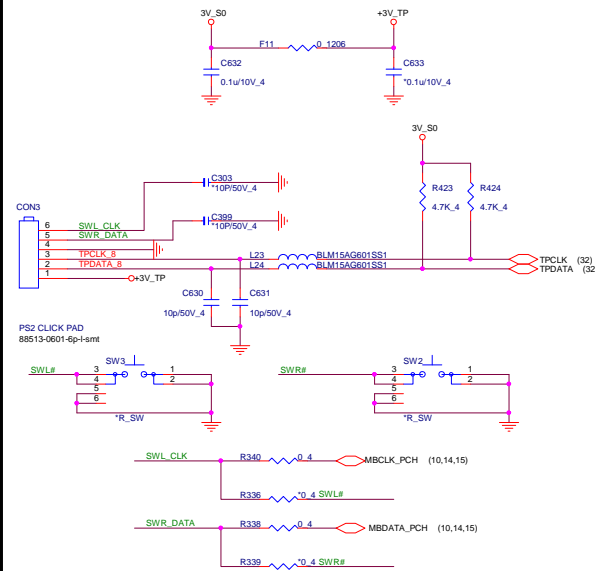
Card reader RTS5229



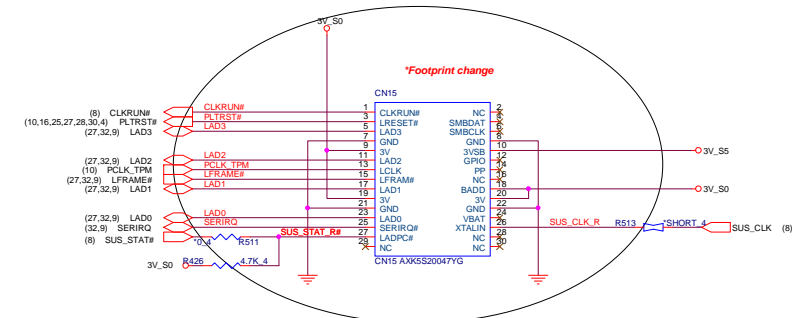
INT KeyBoard



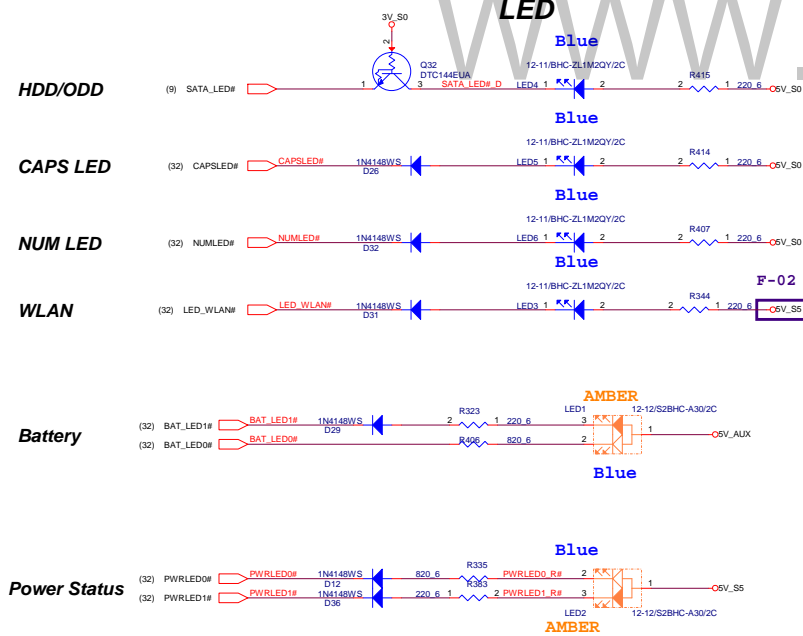
Touch Pad / Click PAD



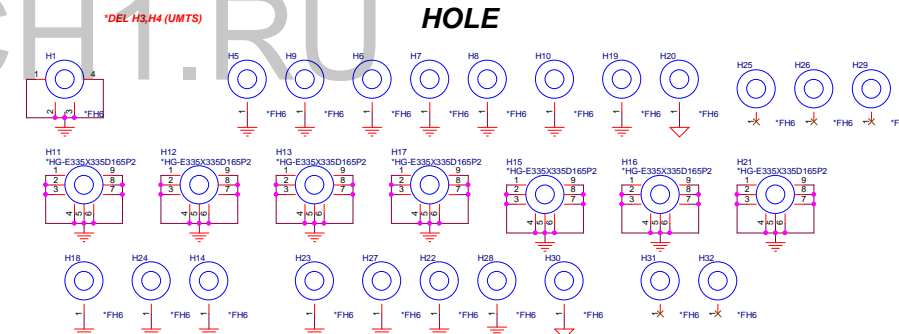
TPM Connector



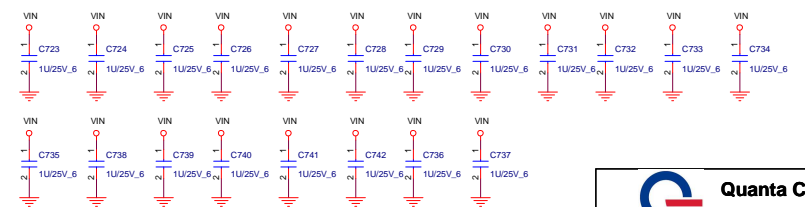
LED



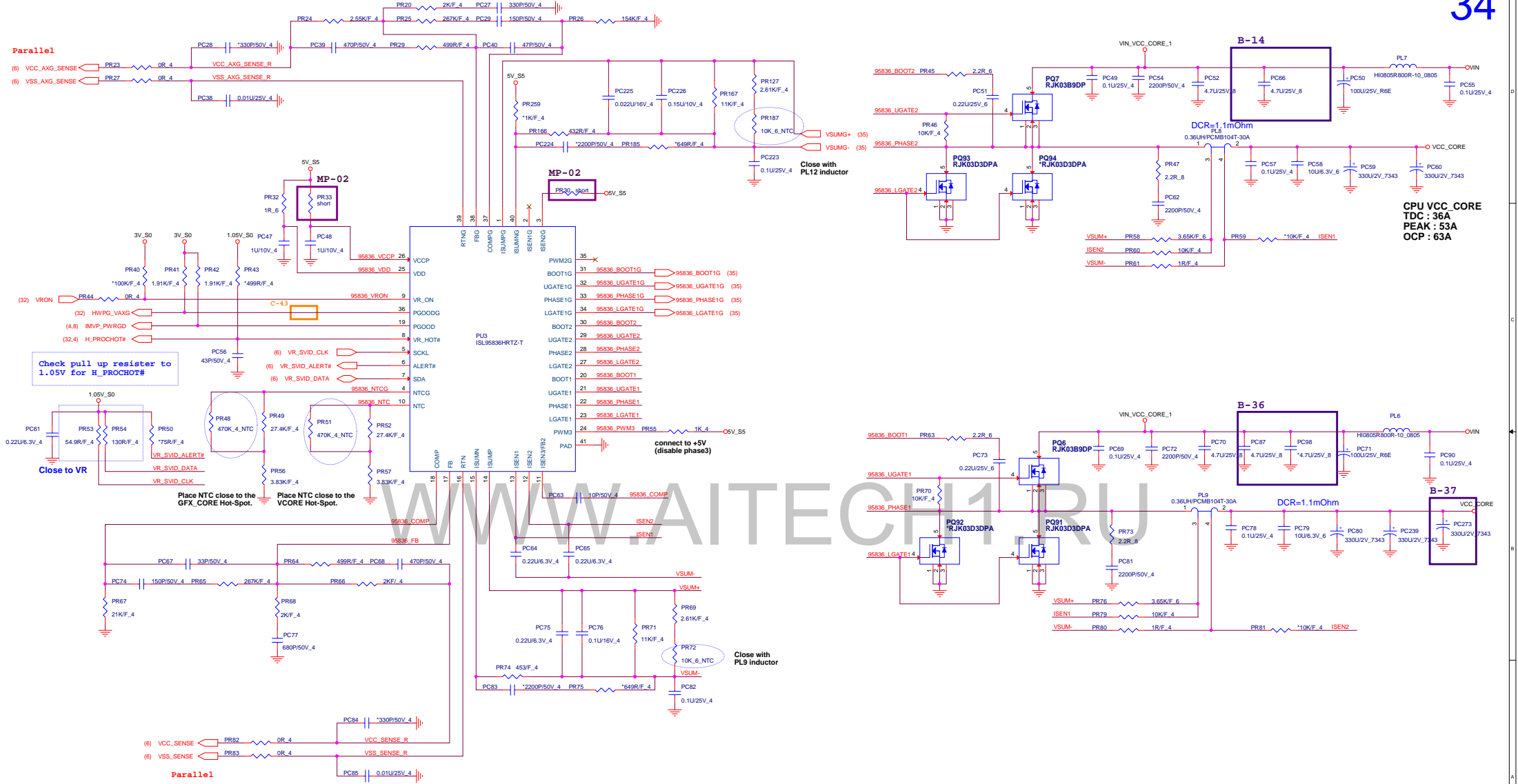
HOLE



Decoupling Cap

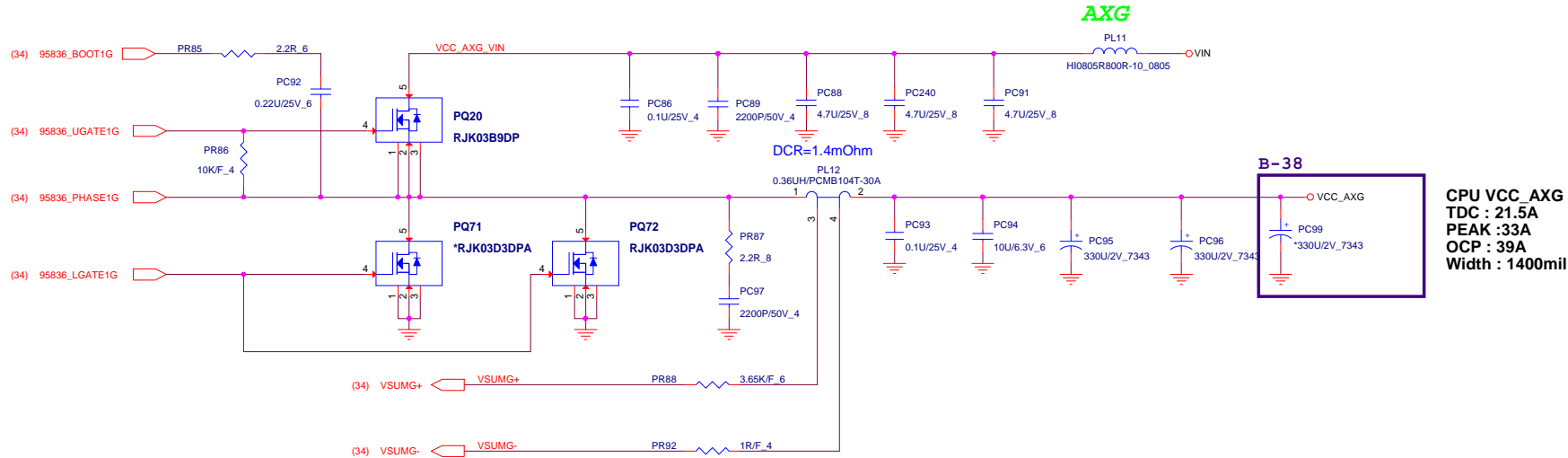


CPU VCORE (ISL95836HRTZ-T and ISL6208CRZ-T)



Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	CYN	CV+36V0MZ13	30	50	1.4m Max.	10x10x4	PCMB104T-R36MT
0.36uH 20%	Panasonic	CV+18V0MZ04	30	34	1.4m Max.	10x10x4	ETQP4LR36WFC




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Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size	Vendor P/N
0.36uH 20%	Panasonic	CV+36Q0MZ00	20	25	1.4m Max.	7X7X4	ETQP4LR36AFM

L/S Mosfet parameter

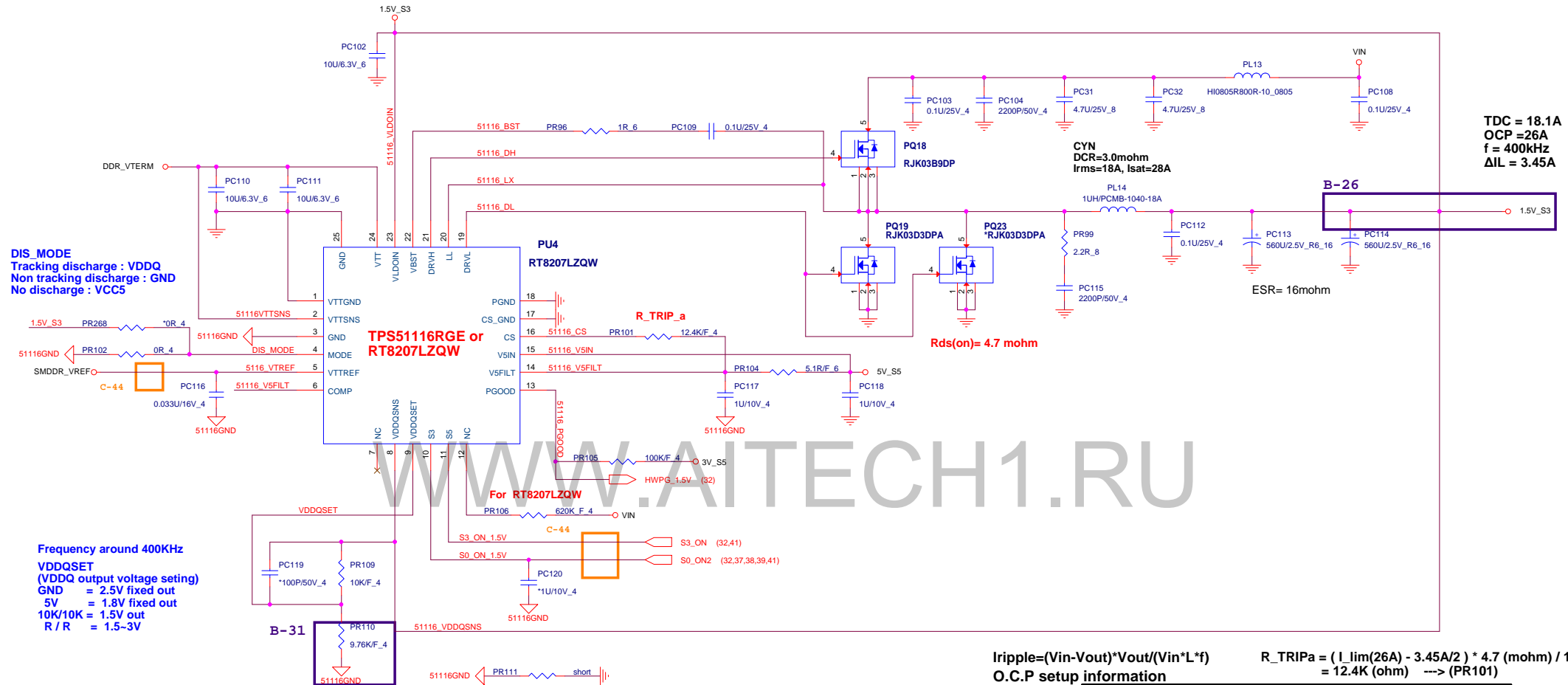
Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
RJK03D3DPA	P_PAK	20A/40A	4.7m	YES
AOL1718	P_PAK	20A/90A	4.3m	YES
RMW200N03FUB	P_PAK	20A/80A	4.6m	NO
FDMS0310S	P_PAK	14A/83A	5.2m	YES

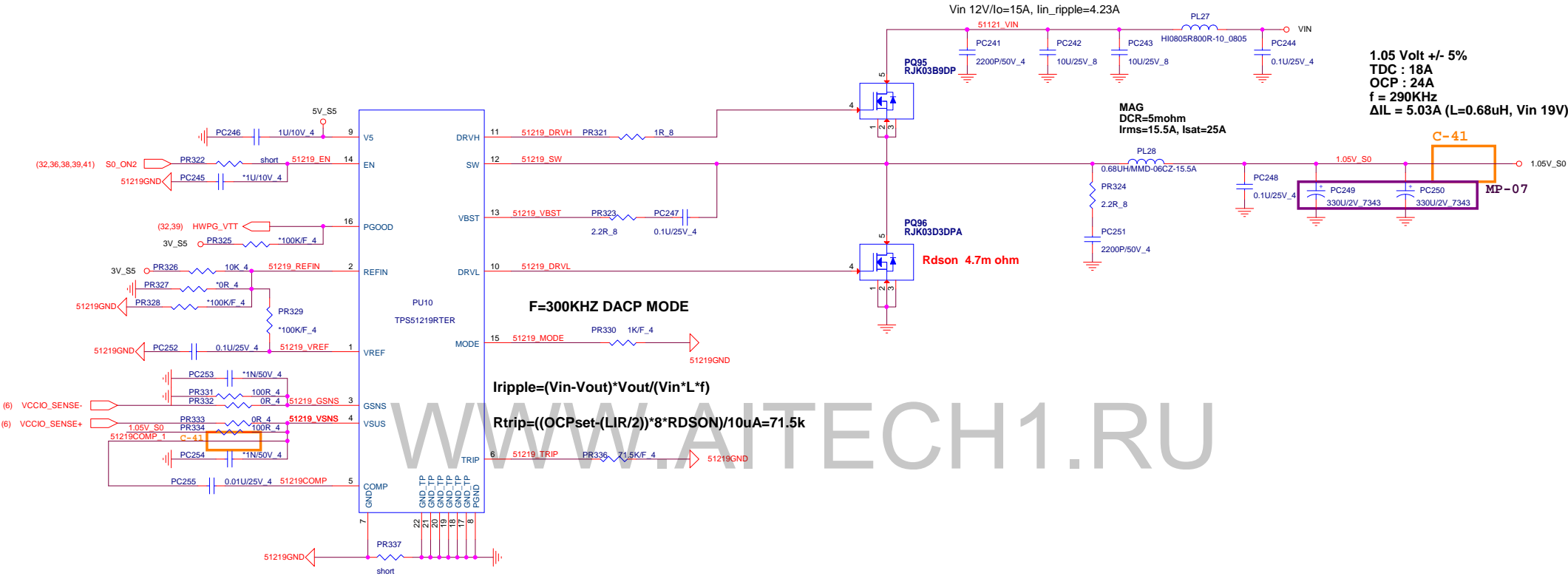


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CPU GFX (ISL95836HRTZ-T)

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DDR3 1.5V_S3 (TPS51116RGE or RT8207LZQW)





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Output Voltage Selection

RFIN=3.3V	output voltage=1.05V
RFIN=GND	output voltage=1.00V
Resister Divider	Adjustable from VREF

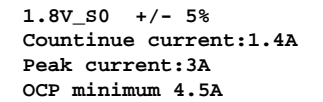
Inductor information

Value	Vendor	QCI P/N	Irms(A)	Isat(A)	Rdc (ohm)	Size
1uH 20%	CYN	CV-10I0MZ04	18	28	3.3m Max.	11X10X4
1uH 20%	MAG Layer	CV-10L0MZ28	21	30	3.1m Max.	11X10X4

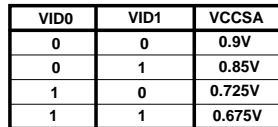
O.C.P setup information

Output	Mos Rds_on	I_OCP	OC_ΔIL(A)	Freq(KHz)	Inductor	R_TRIP
1.05V	4.3m_Max	24	3.306	300	1uH	56.2K

VCCIO_SENSE- connect to the GND sense point of the load
VCCIO_SENSE+ connect to the load voltage sense point.

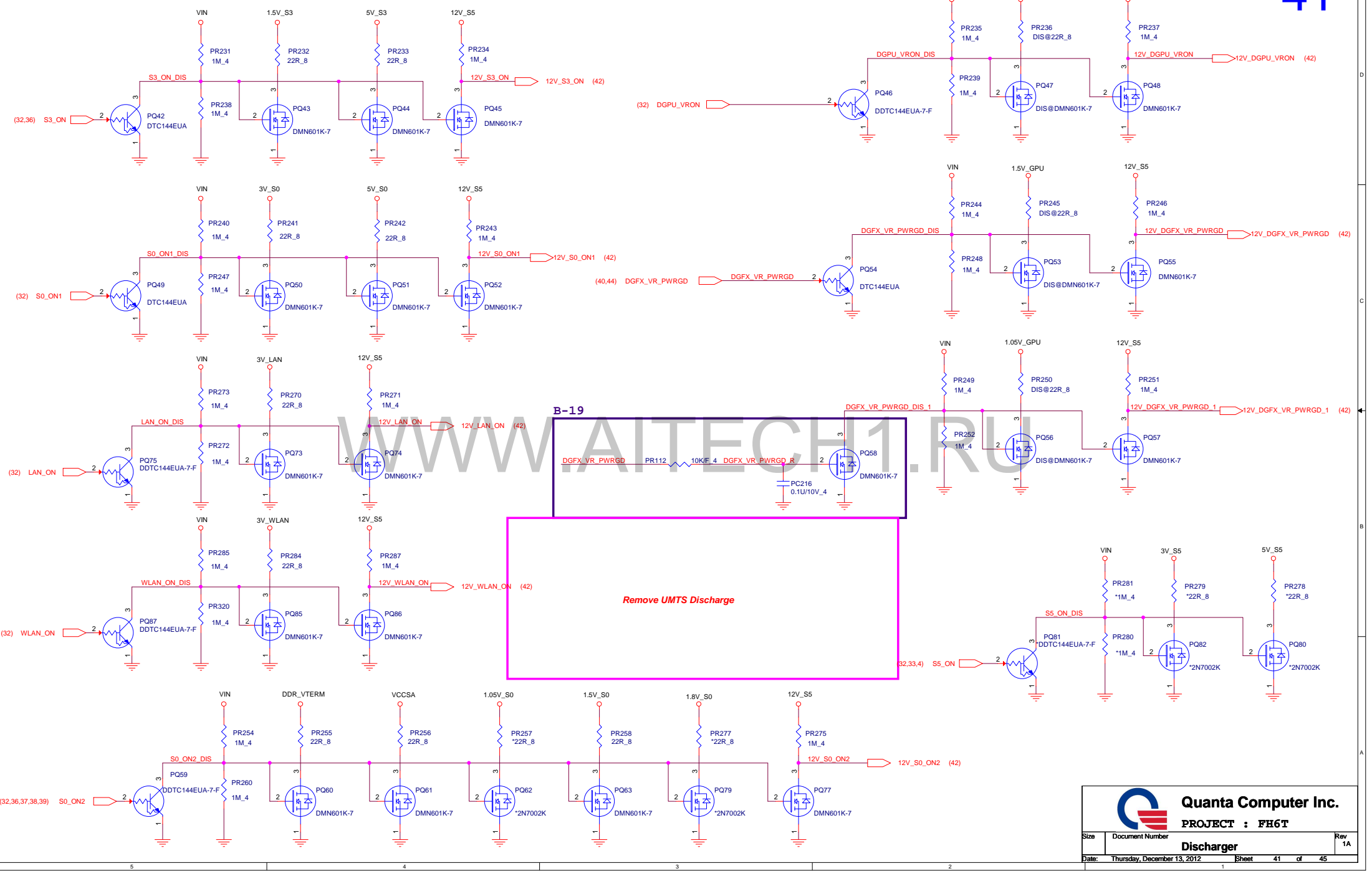


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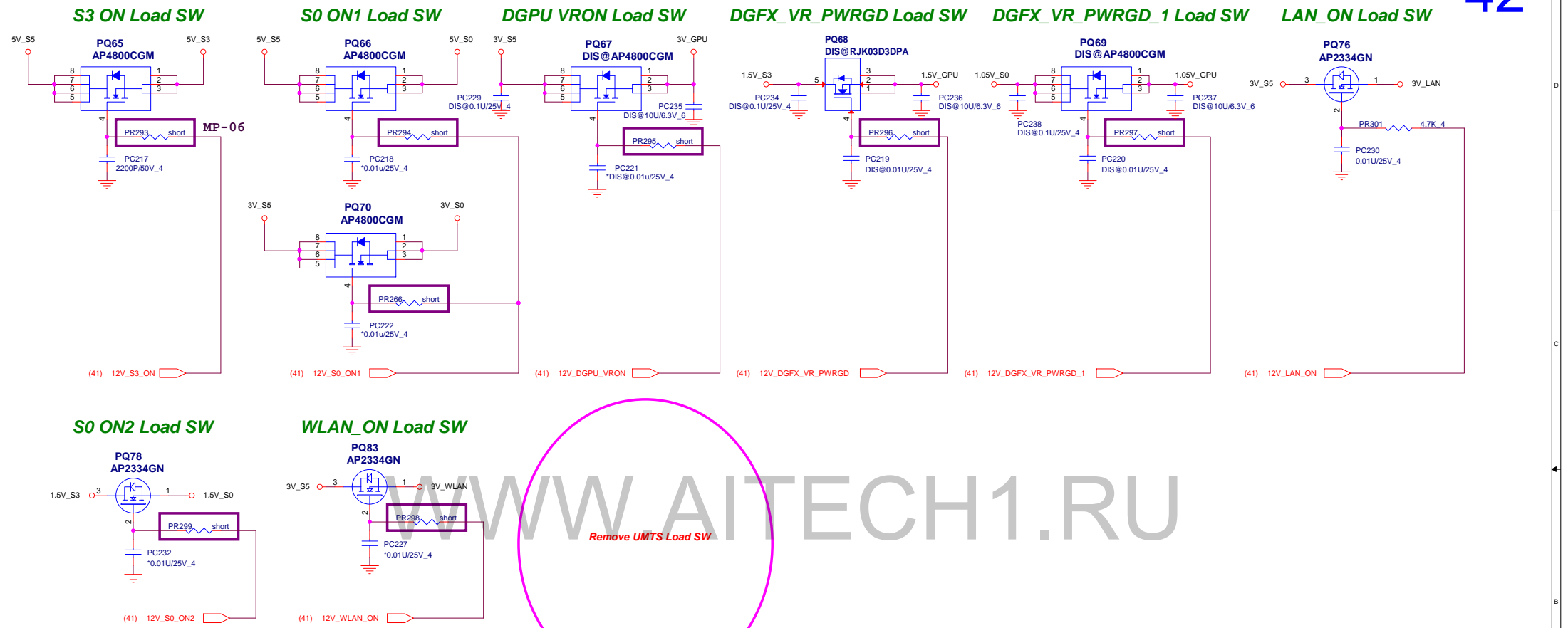


Power rail discharge

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Load Switch

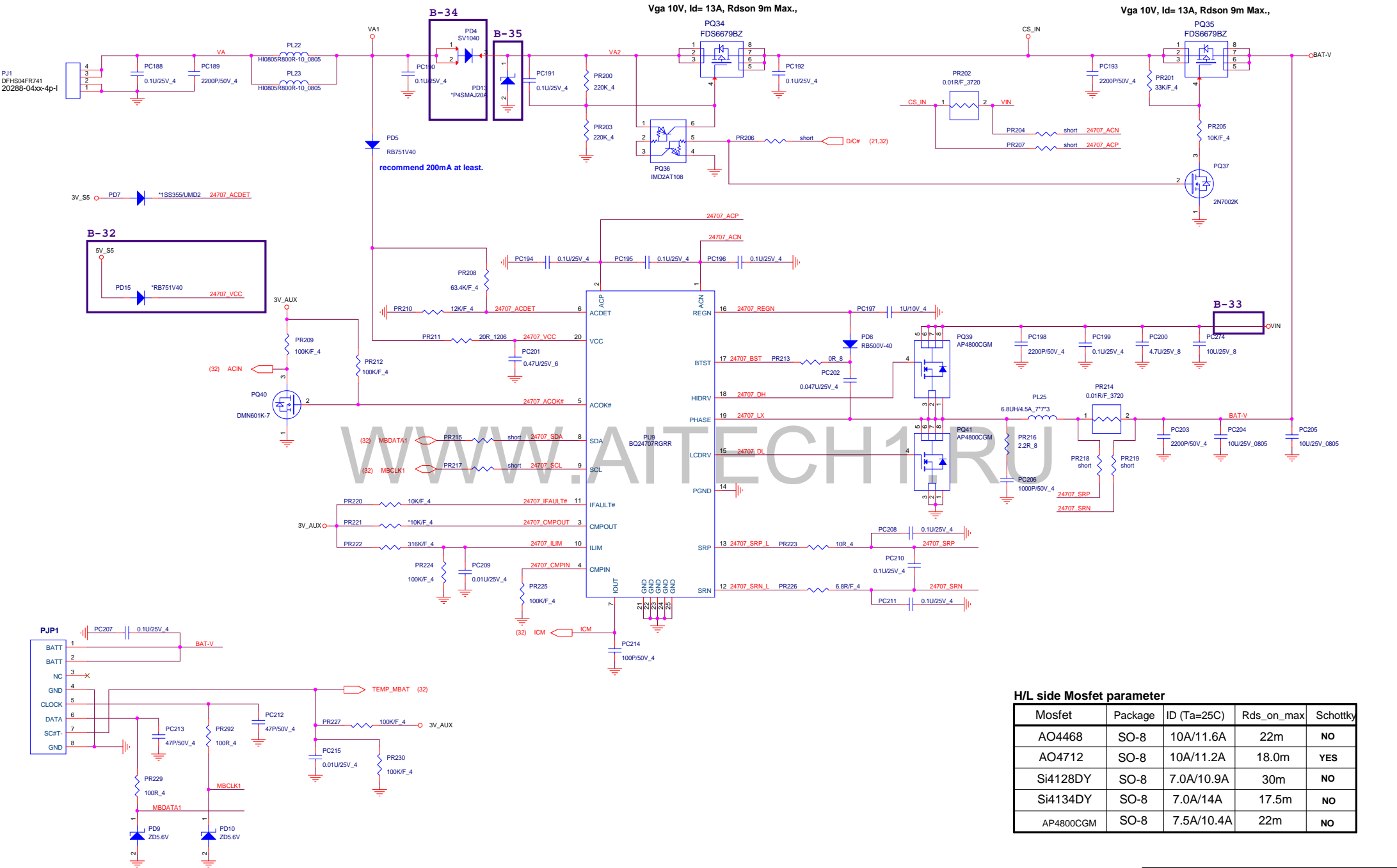


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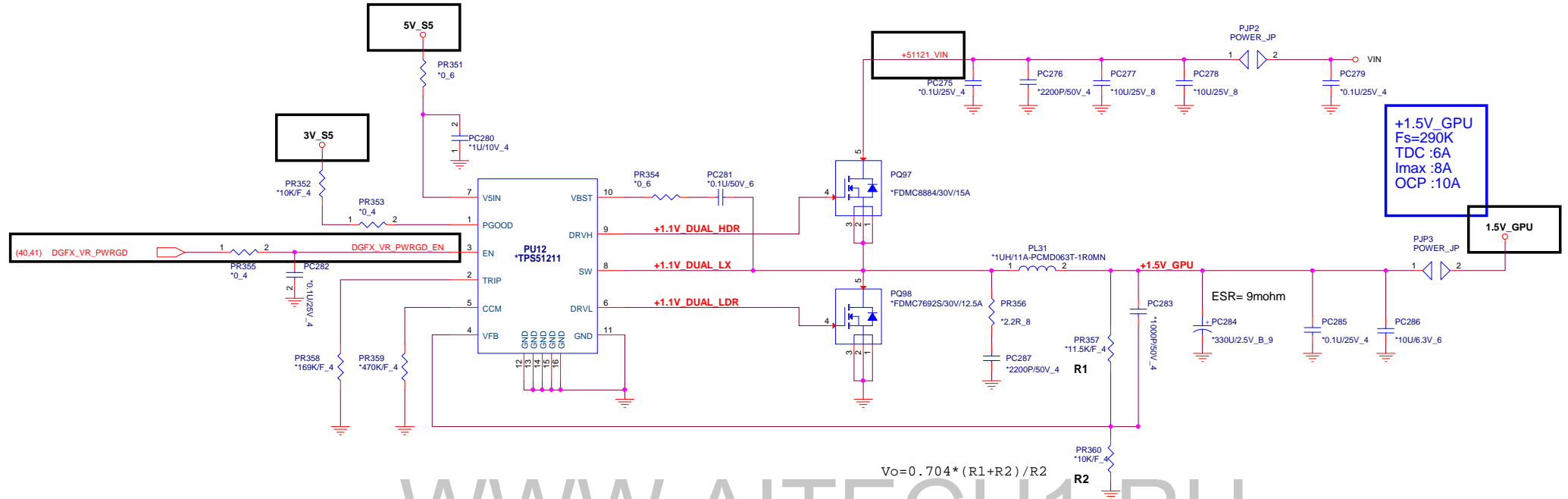
Remove UMTS Load SW

Mosfet parameter

Mosfet	Package	ID(Ta=25C)	Rds_on_max	Vgs_max
AO4468	SO-8	8.4A/10.4A	22m	+/- 20V
AP4800CGM	SO-8	7.5A/10.4A	22m	+/- 20V
Si4128DY	SO-8	7.0A/10.9A	30m	+/- 20V
Si4134DY	SO-8	7.0A/14A	17.5m	+/- 20V
ME3424D	TSOP-6	5.0A/6.7A	42m	+/- 20V
AP2334GN	SOT-23	4.5A/5.0A	42m	+/- 20V
AO3404	SOT-23	5.0A/5.8A	43m	+/- 20V



H/L side Mosfet parameter				
Mosfet	Package	ID (Ta=25C)	Rds_on_max	Schottky
AO4468	SO-8	10A/11.6A	22m	NO
AO4712	SO-8	10A/11.2A	18.0m	YES
Si4128DY	SO-8	7.0A/10.9A	30m	NO
Si4134DY	SO-8	7.0A/14A	17.5m	NO
AP4800CGM	SO-8	7.5A/10.4A	22m	NO



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Quanta Computer Inc.

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+1.5V_GPU

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FH6T Mother Board Schematics Revision History

PCB Rev	Sch Rev	BOM Rev	DATE	Change List & Description
A	01	-		1st Release A - B
B	02	-		
C	03	-	Dec/22/12'	B - C
MP				C - MP1


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Change List
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